

-40V P-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ◇ Advanced TRENCH cell design
- ◇ Surface-mounted package
- ◇ Low gate charge

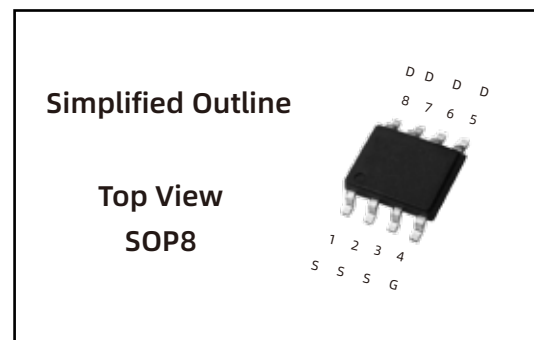
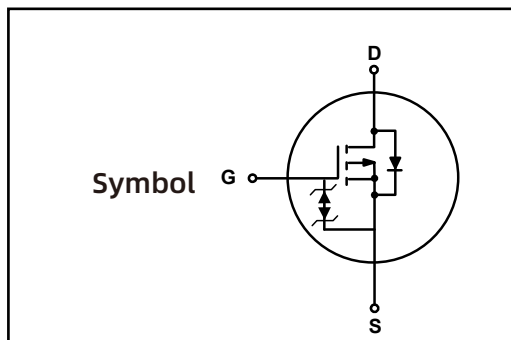
1.2 Applications

- ◇ Motor driver appliances
- ◇ High power inverter system
- ◇ Adapter appliances

1.3 Quick reference

- ◇ $BV \cong -40\text{ V}$
- ◇ $P_{\text{tot}} \cong 2\text{ W}$
- ◇ $I_D \cong -5.7\text{ A}$
- ◇ $R_{\text{DS(ON)}} \cong 55\text{ m}\Omega @ V_{\text{GS}} = -10\text{ V}$
- ◇ $R_{\text{DS(ON)}} \cong 80\text{ m}\Omega @ V_{\text{GS}} = -4.5\text{ V}$

2. Pin Description



3. Marking Information

Product Name	Marking
LN480P040S	LN480P040S CYWWZZ XXXXXX

4.Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_A = 25\text{ }^{\circ}\text{C}$	-40	-	V
V_{GS}	Gate-Source Voltage	$T_A = 25\text{ }^{\circ}\text{C}$	-	± 20	V
I_D^*	Drain Current (DC)	$T_A = 25\text{ }^{\circ}\text{C}, V_{GS} = -10\text{ V}$	-	- 5.7	A
		$T_A = 100\text{ }^{\circ}\text{C}, V_{GS} = -10\text{ V}$		- 3	A
$I_{DM}^{*,**}$	Drain Current (Pulsed)	$T_A = 25\text{ }^{\circ}\text{C}, V_{GS} = -10\text{ V}$	-	- 18.8	A
P_{tot}^*	Total Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	-	2	W
T_{stg}	Storage Temperature		- 55	150	$^{\circ}\text{C}$
T_J	Junction Temperature		-	150	$^{\circ}\text{C}$
$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient		-	56	$^{\circ}\text{C}/\text{W}$

Notes :

* Surface Mounted on 1 in² pad area, t ≤ 10 sec

** Pulse width ≤ 300 μs, duty cycle ≤ 2 %

*** limited by bonding wire

5.Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
LN480P040S	SOP8	Ø330mm	12mm	3000	

Note: COMTECH defines “ Green ” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

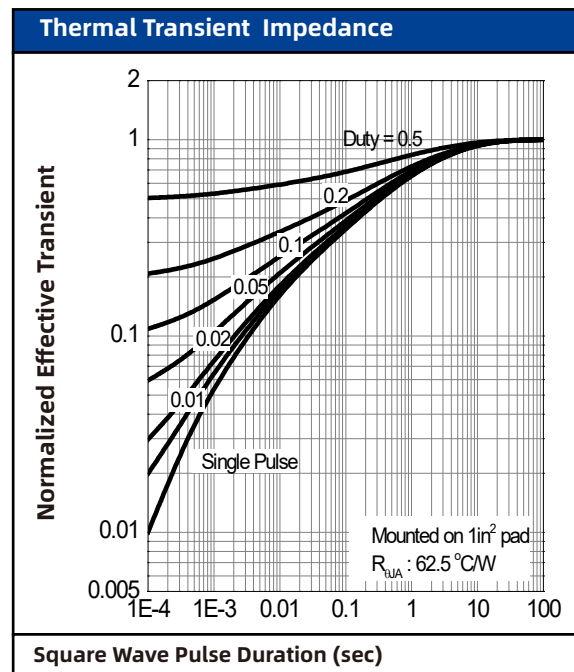
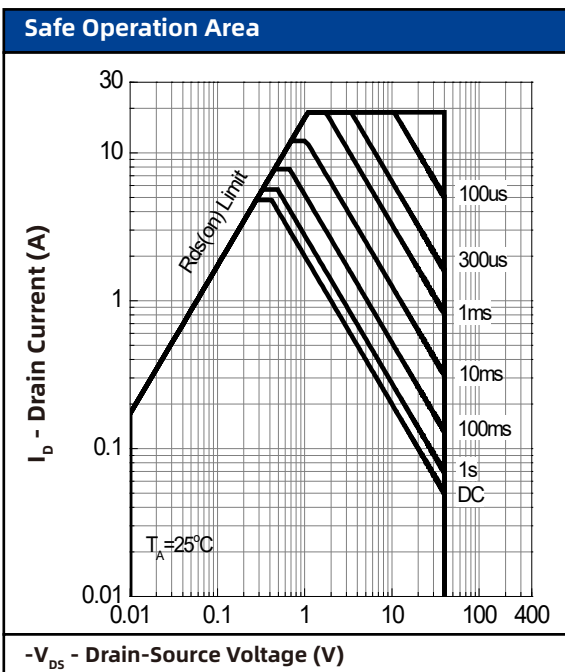
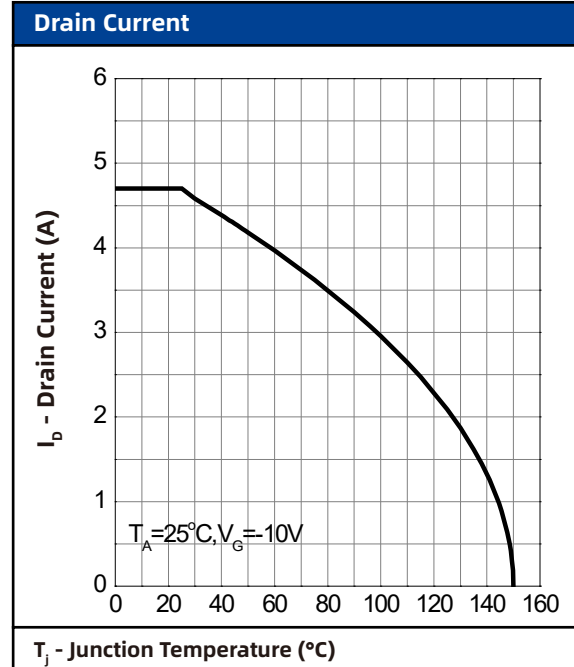
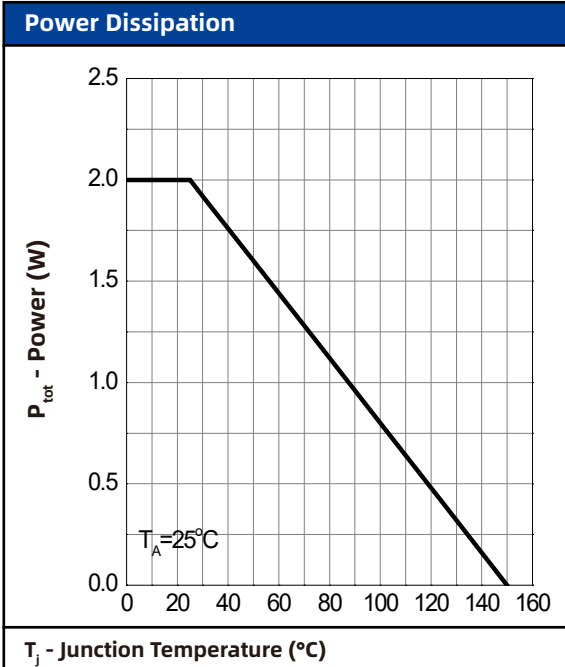
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = -250\ \mu\text{A}$	- 40	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = -250\ \mu\text{A}$	- 1	-	- 2	V
I_{DSS}	Drain Leakage Current	$V_{DS} = -32\text{ V}, V_{GS} = 0\text{ V}$	-	-	- 1	μA
I_{GSS}	Gate Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	± 8	nA
$R_{DS(on)}^a$	Channel On-State Resistance	$V_{GS} = -10\text{ V}, I_D = -4\text{ A}$	-	48	55	m Ω
		$V_{GS} = -4.5\text{ V}, I_D = -2\text{ A}$	-	71	80	
Diode Characteristics						
V_{SD}^a	Diode Forward Voltage	$I_{SD} = -4\text{ A}, V_{GS} = 0\text{ V}$	-	-	-1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = -4\text{ A}$	-	11	-	nS
Q_{rr}	Reverse Recovery Charge	$dI_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	6.9	-	nC
Dynamic Characteristics^b						
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = -20\text{ V}$ Frequency = 1 MHz	-	783	-	pF
C_{OSS}	Output Capacitance		-	60	-	
C_{rSS}	Reverse Transfer Capacitance		-	52	-	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = -20\text{ V}, V_{GEN} = -10\text{ V},$ $R_G = 3.9\ \Omega, R_L = 5\ \Omega,$ $I_{DS} = -4\text{ A}$	-	5.8	-	nS
t_r	Turn-on Rise Time		-	31	-	
$t_d(off)$	Turn-off Delay Time		-	149	-	
t_f	Turn-off Fall Time		-	75	-	
Gate Charge Characteristics^b						
Q_g	Total Gate Charge	$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V},$ $I_{DS} = -4\text{ A}$	-	14	-	nC
Q_{gs}	Gate-Source Charge		-	3.8	-	
Q_{gd}	Gate-Drain Charge		-	1.8	-	

Notes :

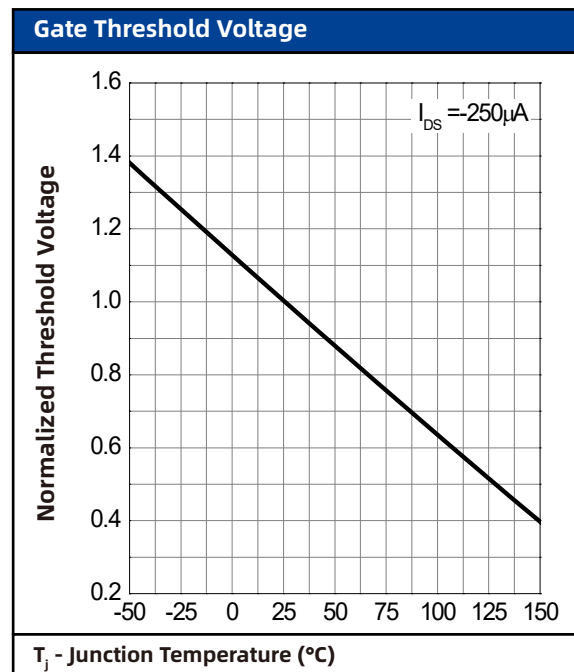
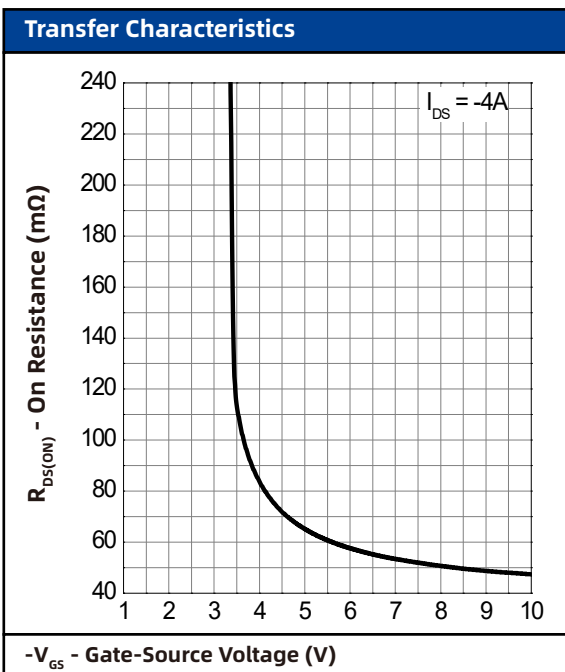
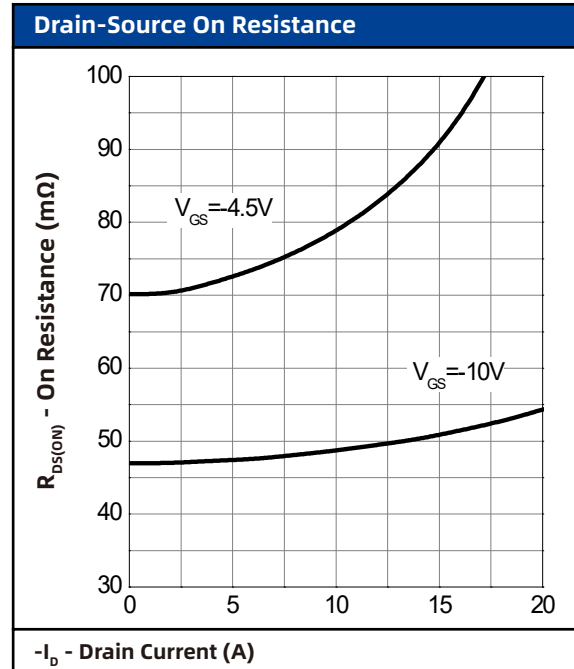
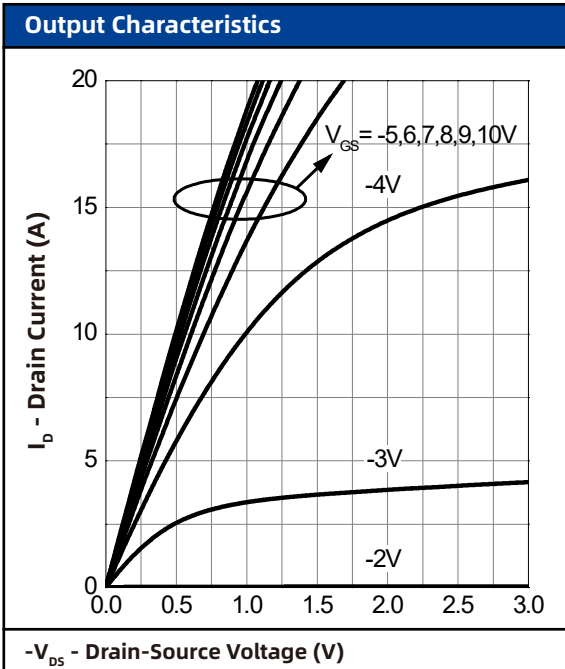
a : Pulse test ; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

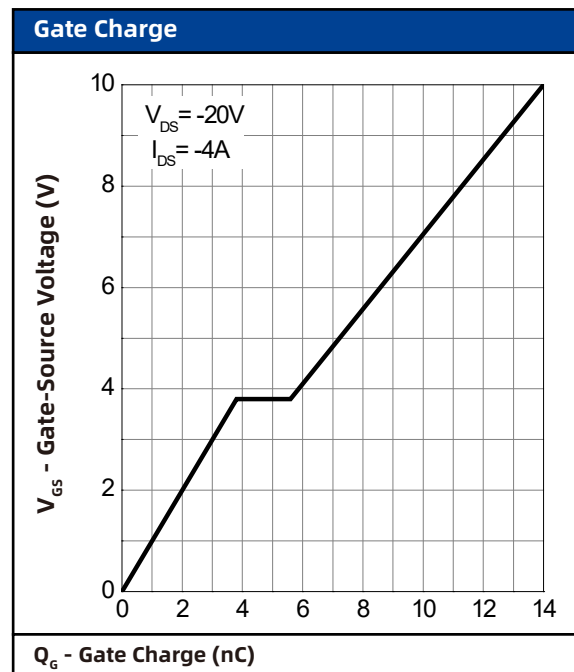
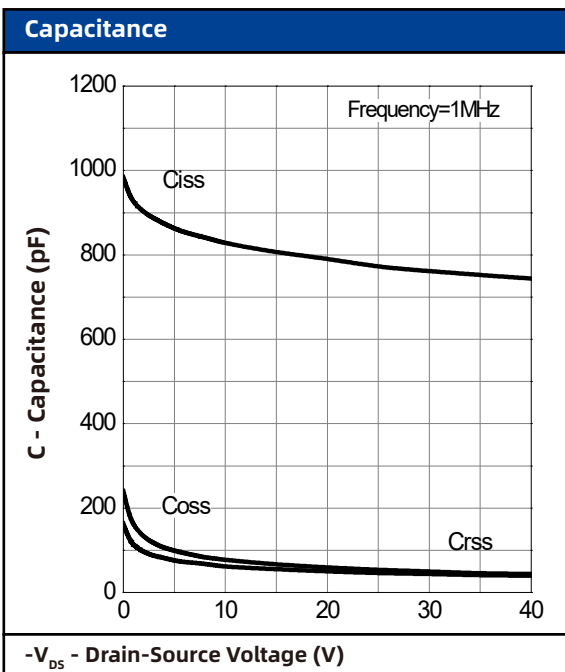
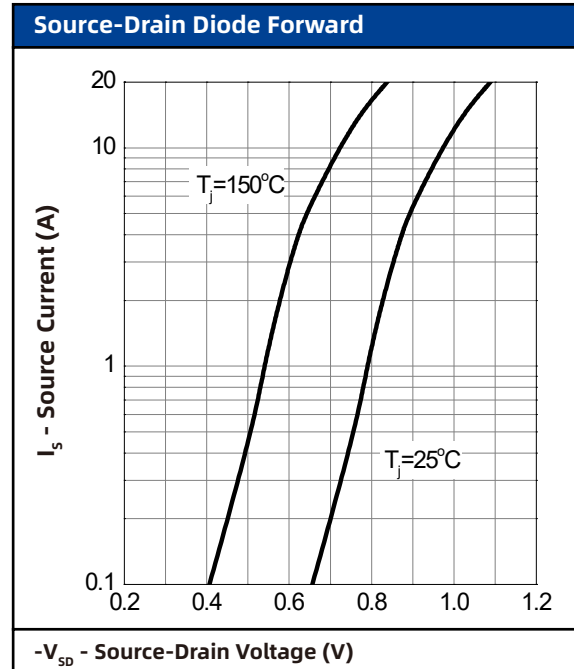
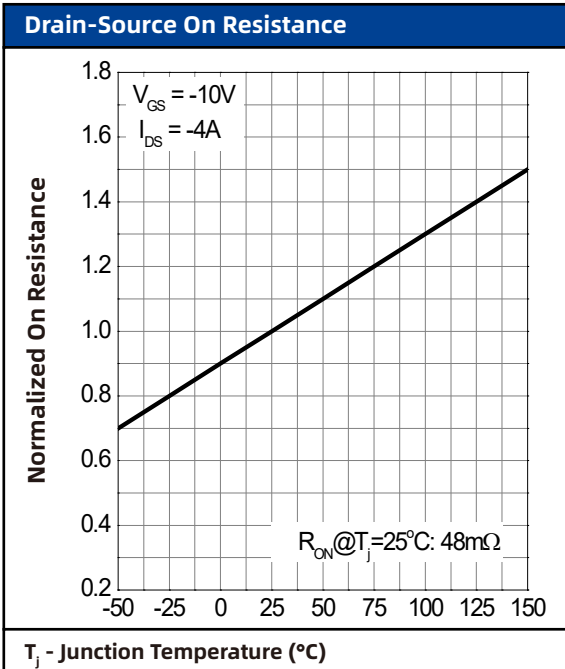
7. Typical Characteristics



7. Typical Characteristics (cont.)

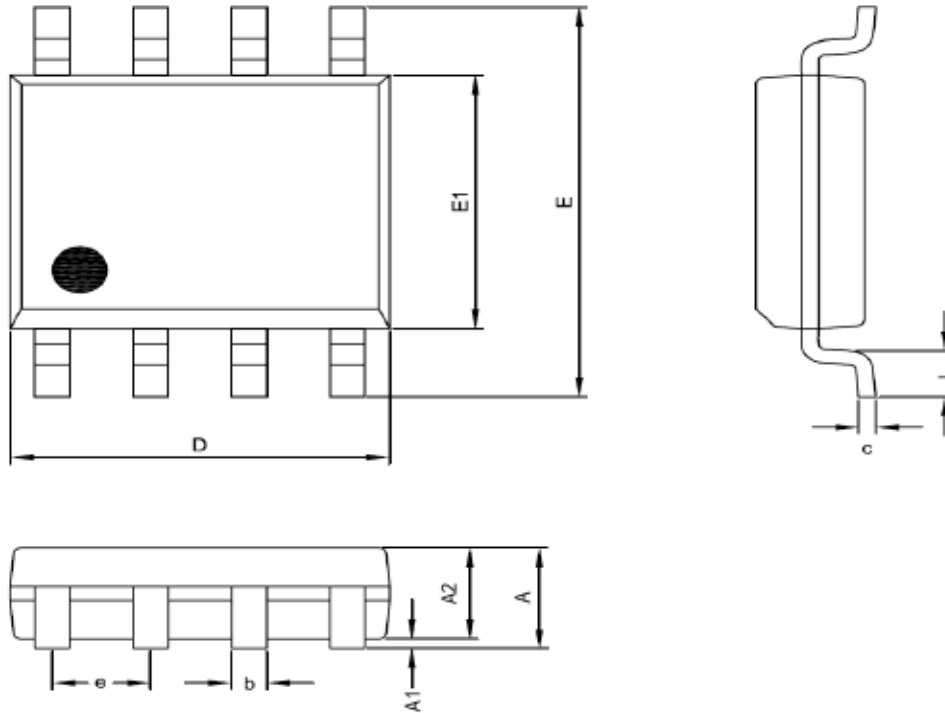


7. Typical Characteristics (cont.)



8. Package Dimensions

SOP8 Package



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes :

a : Jedec outline:MS-012AA

b : Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side.

c : Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.