

## 40V N-Channel Enhancement Mode MOSFET

### 1. Product Information

#### 1.1 Features

- ◇ Advanced SGT cell design
- ◇ Low Gate Charge
- ◇ Low On-Resistance
- ◇ RoHS and Halogen-Free Compliant
- ◇ 100%  $\Delta V_{DS}$  & UIS & Rg Tested

#### 1.2 Applications

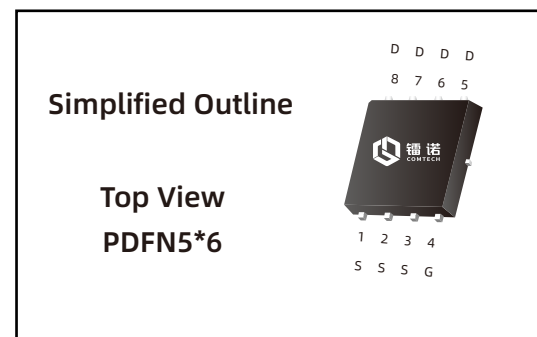
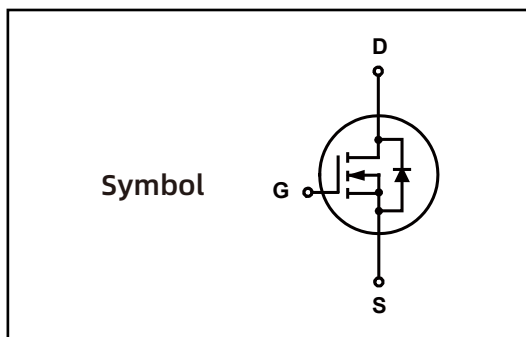
- ◇ DC-DC Converter
- ◇ Drones
- ◇ Motor drivers
- ◇ Light electric vehicles

#### 1.3 Quick reference

- ◇  $BV \cong 40\text{ V}$
- ◇  $P_{tot} \cong 259\text{ W}$
- ◇  $I_D \cong 323\text{ A}$
- ◇  $R_{DS(ON)} \cong 1.8\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- ◇  $R_{DS(ON)} \cong 3.2\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$



### 2. Pin Description



### 3.Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit	Note
$V_{DS}$	Drain-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	40	V	-
$V_{GS}$	Gate-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	$\pm 20$	V	-
$I_D^*$	Drain Current ( DC )	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	323	A	Fig.2
		$T_C = 100\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	229	A	
$I_{DM}^{**},^{***}$	Drain Current ( Pulsed )	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	479	A	-
$P_{tot}$	Drain power dissipation	$T_C = 25\text{ }^\circ\text{C}$	-	259	W	Fig.1
		$T_C = 100\text{ }^\circ\text{C}$	-	129	W	
$T_{stg}$	Storage Temperature		-55	175	$^\circ\text{C}$	-
$T_J$	Junction Temperature		-	175	$^\circ\text{C}$	-
$I_S$	Continuous-Source Current	$T_C = 25\text{ }^\circ\text{C}$	-	323	A	-
$E_{AS}^*$	Single Pulsed Avalanche Energy	$V_{DD} = 40\text{ V}, L = 0.1\text{ mH}$	-	207	mJ	Fig.19

### 4.Thermal Characteristics

$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient	-	27	$^\circ\text{C/W}$	Fig.16
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case	-	0.58		

Notes :

\* Surface Mounted on 1 in<sup>2</sup> pad area,  $t \leq 10\text{ sec}$

\*\* Pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$

\*\*\* limited by bonding wire

### 5.Marking Information

Product Name	Package	Reel size	Tape width	Quantity	Note
LN018N040G	PDFN5*6	330mm	12mm	5000	

Note: COMTECH defines " Green " as lead-free ( RoHS compliant ) and halogen free ( Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C )

## 6. Electrical Characteristics ( $T_A=25^\circ$ Unless Otherwise Noted )

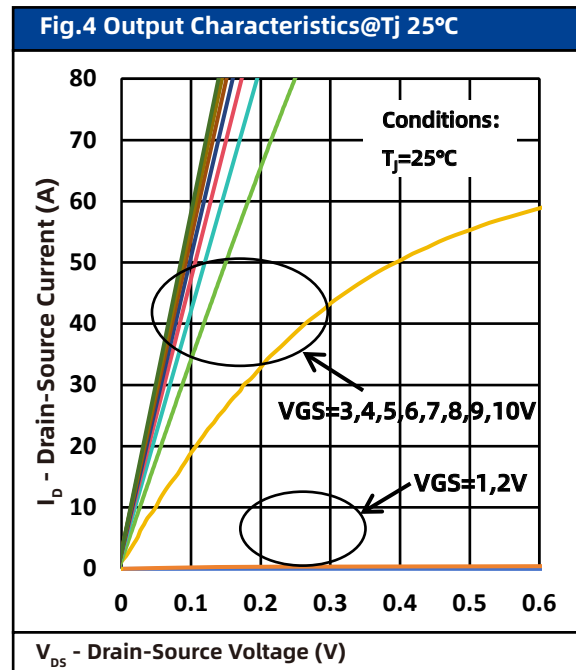
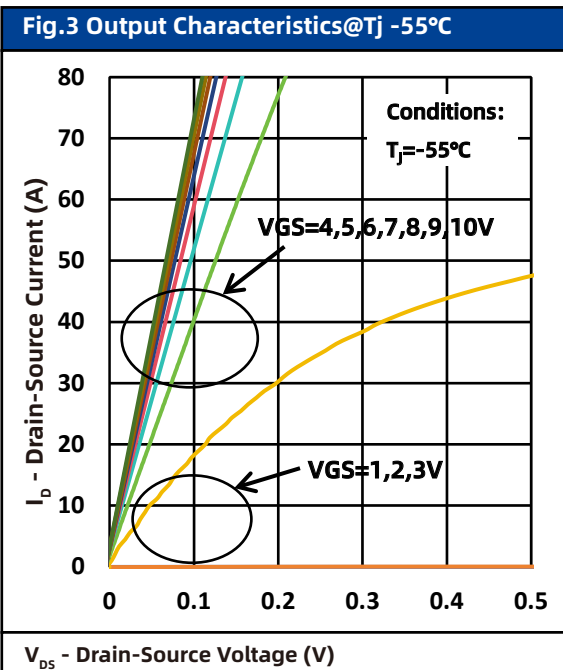
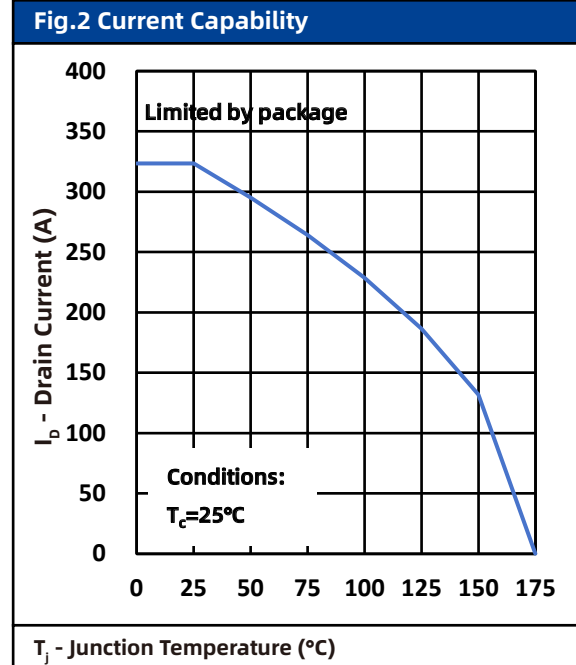
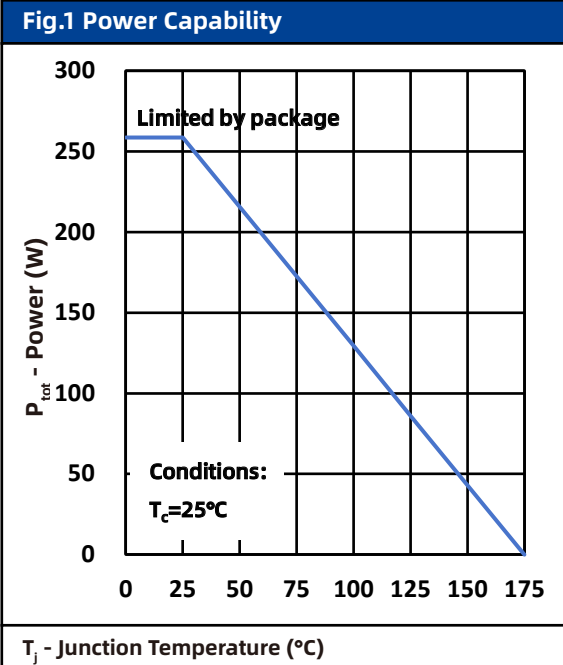
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
<b>Static Characteristics</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	40	-	-	V	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	1	-	3	V	
$I_{DSS}$	Drain Leakage Current	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$	
$I_{GSS}$	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA	
$R_{DS(on)}^a$	On-State Resistance	$V_{GS} = 10\text{ V}, I_{DS} = 50\text{ A}$	-	1.6	1.8	m $\Omega$	Fig.8
		$V_{GS} = 4.5\text{ V}, I_{DS} = 30\text{ A}$	-	2.6	3.2		
<b>Diode Characteristics</b>							
$V_{SD}^a$	Diode Forward Voltage	$I_{SD} = 50\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V	Fig.7
$t_{rr}$	Reverse Recovery Time	$I_{DS} = 50\text{ A}, V_{GS} = 0\text{ V}$	-	77	-	nS	Fig.20
$Q_{rr}$	Reverse Recovery Charge	$di_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	164	-	nC	
<b>Dynamic Characteristics<sup>b</sup></b>							
$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$ Frequency = 1 MHz	-	2370	-	pF	Fig.10
$C_{OSS}$	Output Capacitance		-	453	-		
$C_{rSS}$	Reverse Transfer Capacitance		-	422	-		
$R_G$	Gate Resistance	F= 1 MHz	-	1.1	-	$\Omega$	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V},$ $R_G=2.7\ \Omega, R_L = 4\ \mu\text{H},$ $I_{DS} = 50\text{ A}$	-	25	-	nS	Fig.18
$t_r$	Turn-on Rise Time		-	192	-		
$t_d(off)$	Turn-off Delay Time		-	85	-		
$t_f$	Turn-off Fall Time		-	80	-		
$dv/dt$	Peak Diode Recovery		-	0.083	-		
$di/dt$	Peak Diode Recovery	-	302	-	A/us		
<b>Gate Charge Characteristics<sup>b</sup></b>							
$Q_g$	Total Gate Charge	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V},$ $I_{DS} = 50\text{ A}$	-	60	-	nC	Fig.9
$Q_{gs}$	Gate-Source Charge		-	5	-		
$Q_{gd}$	Gate-Drain Charge		-	25	-		
$V_{plateau}$	Gate plateau voltage		-	2.6	-		

Notes :

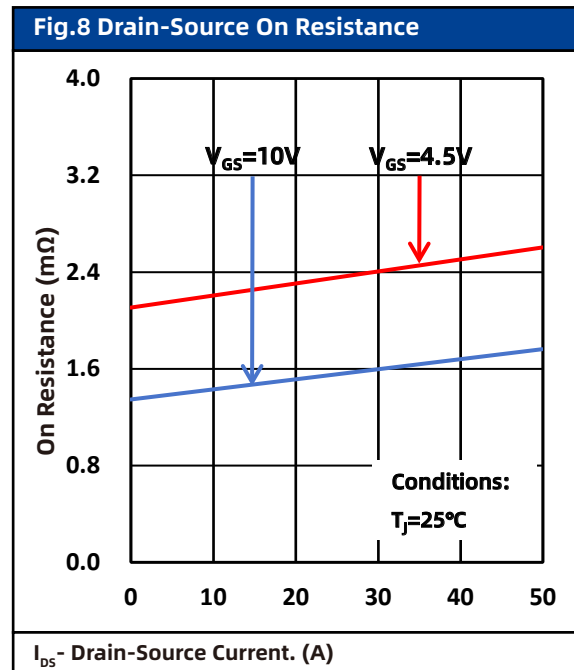
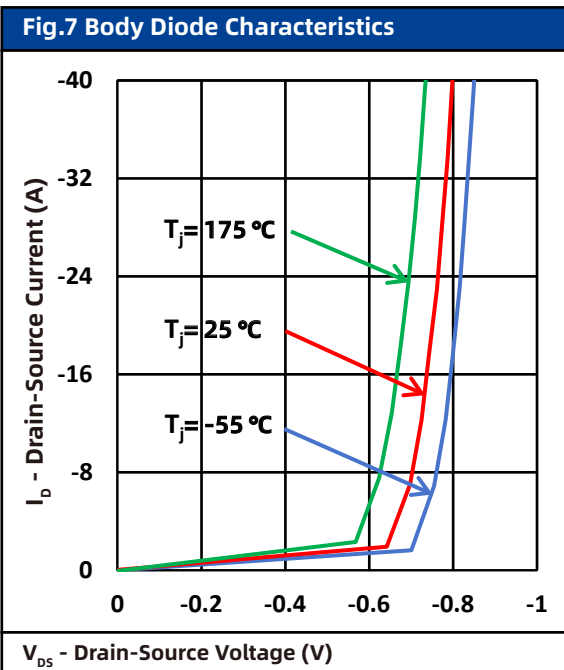
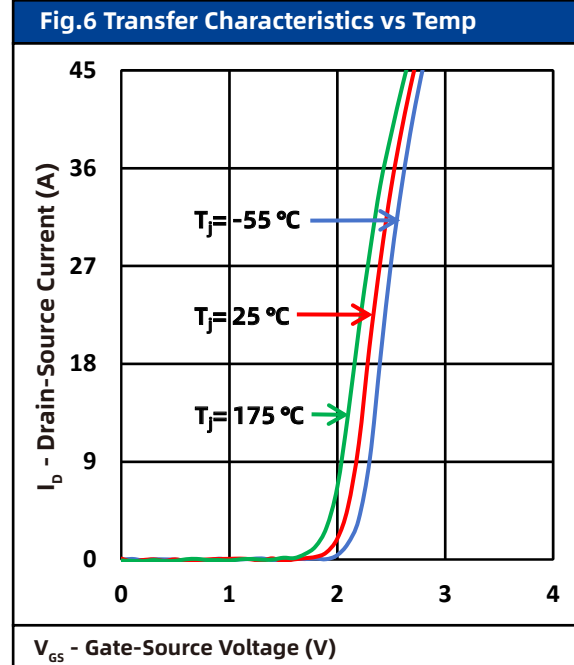
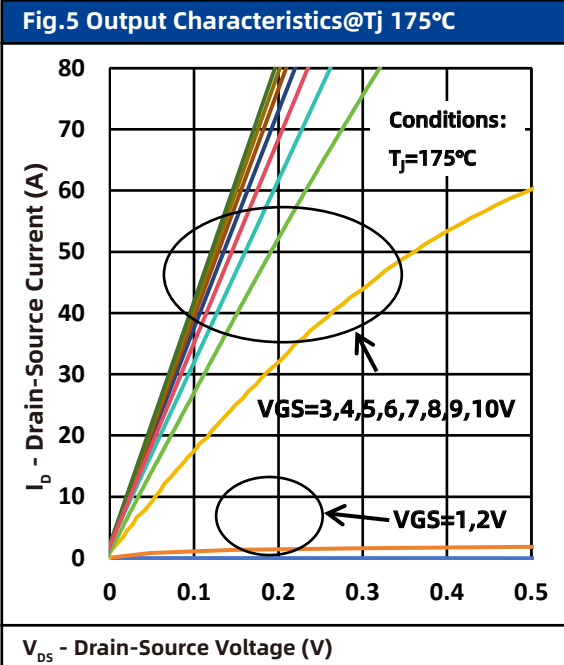
a : Pulse test ; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ 

b : Guaranteed by design, not subject to production testing

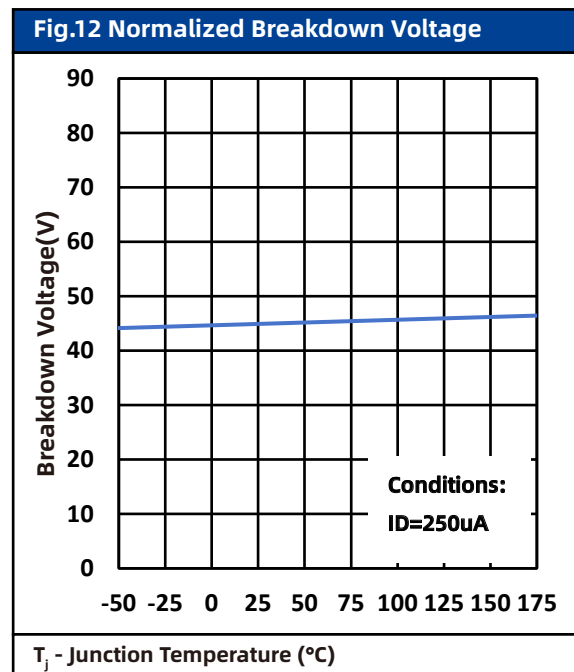
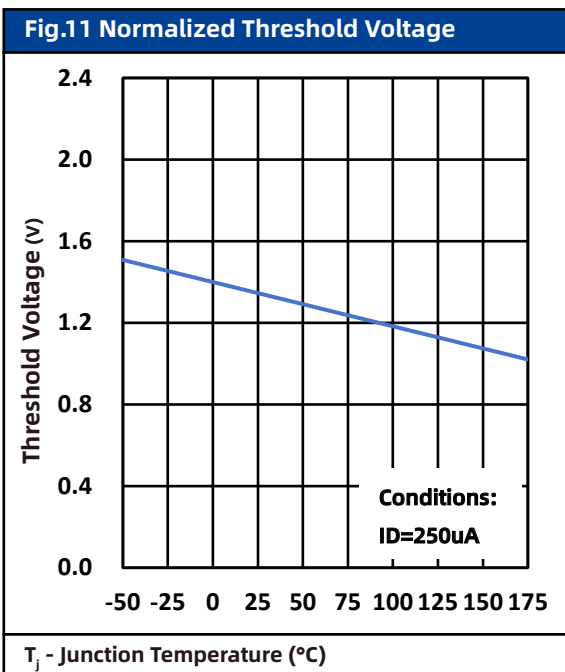
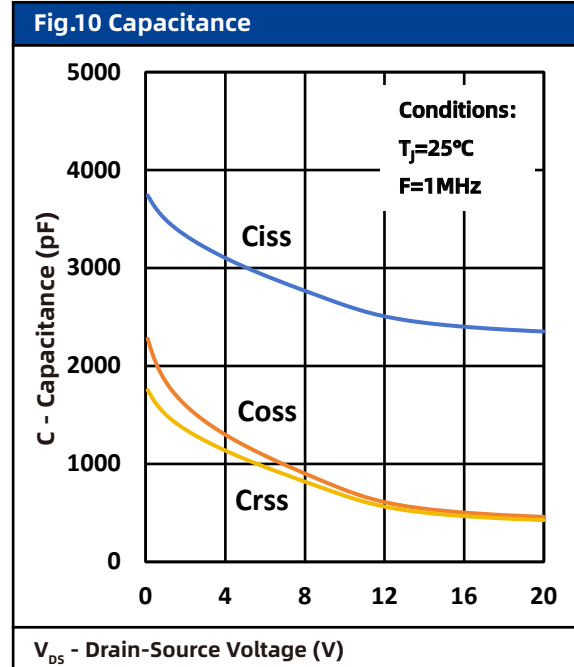
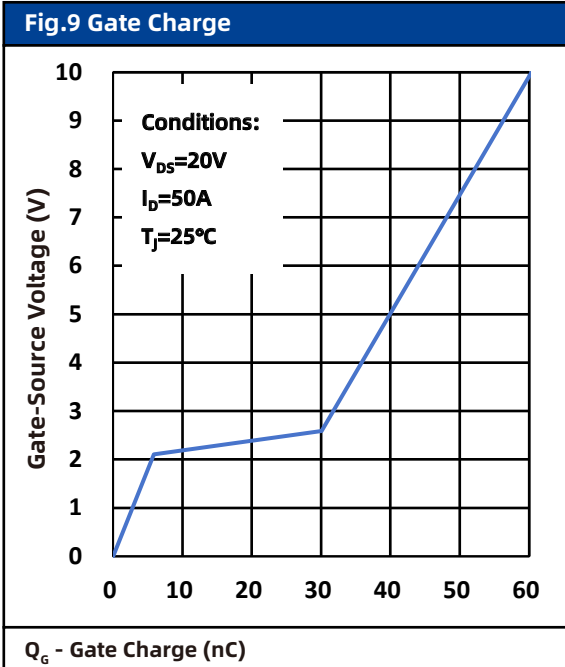
## 7. Typical Characteristics



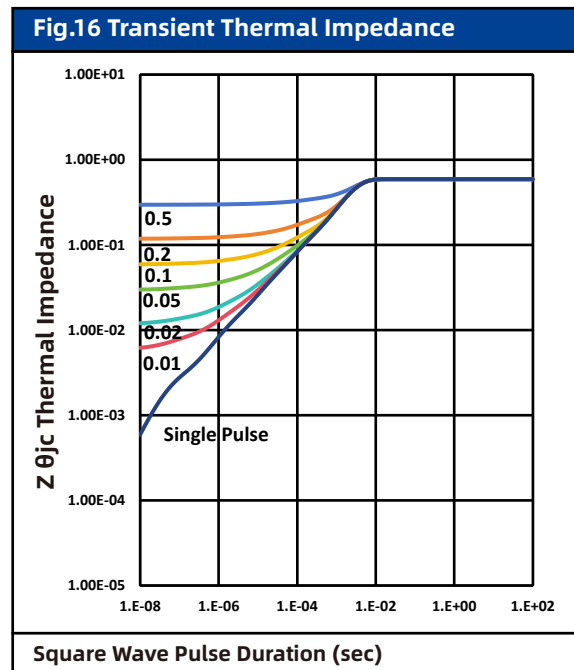
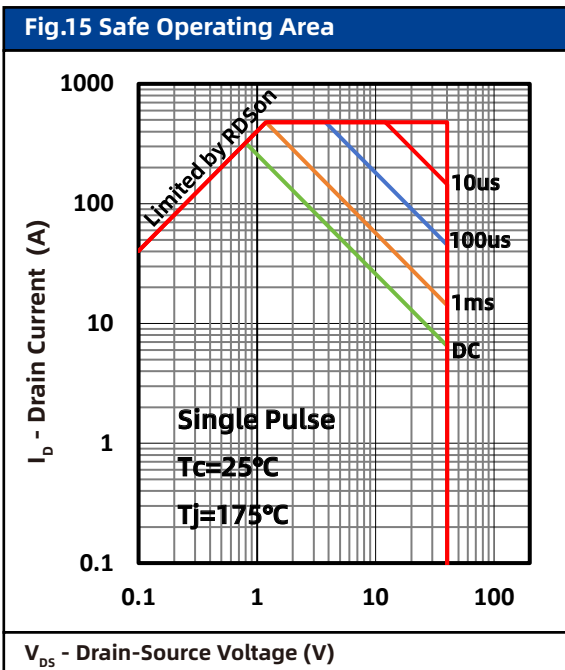
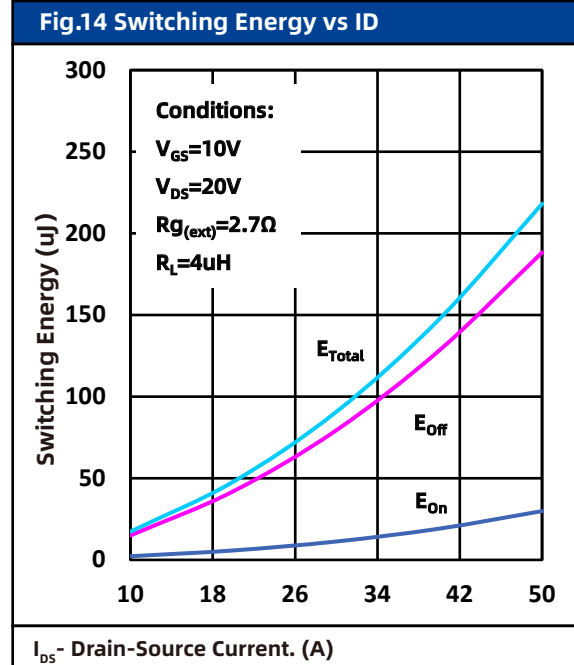
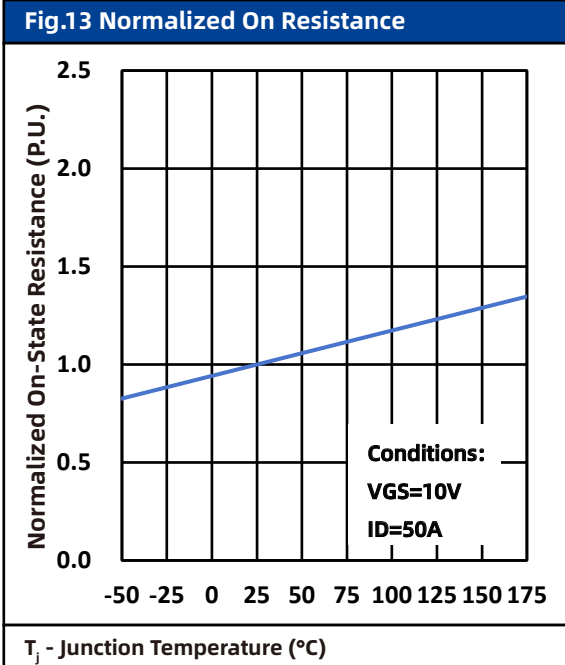
## 7. Typical Characteristics



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Fig.17 Gate Charge Test Circuit & Waveform

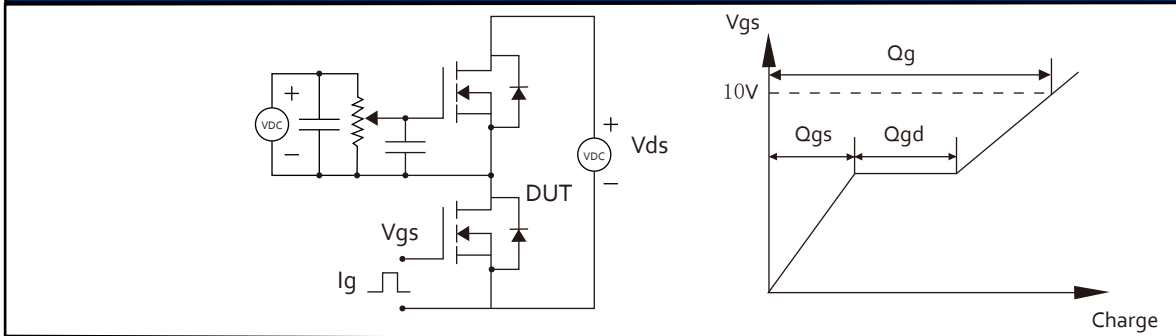


Fig.18 Resistive Switching Test Circuit & Waveforms

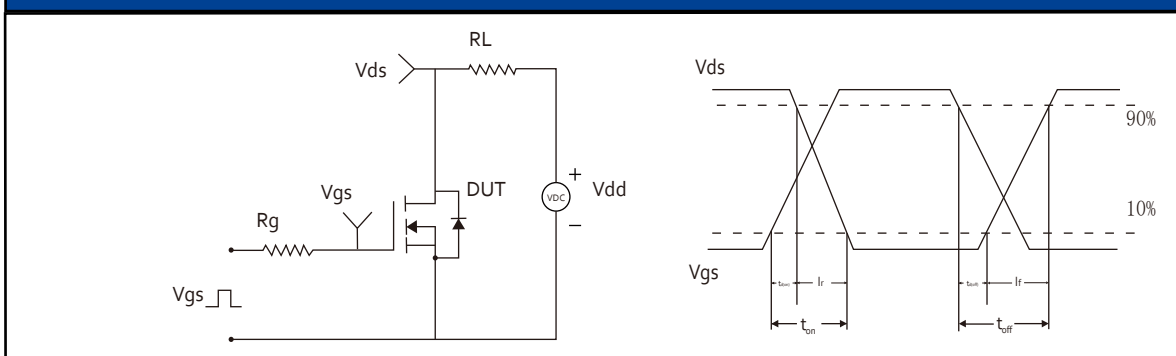


Fig.19 Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

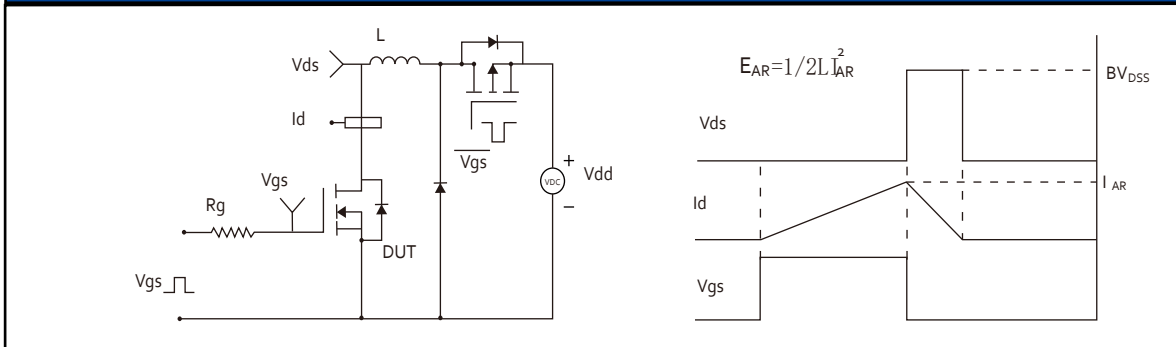
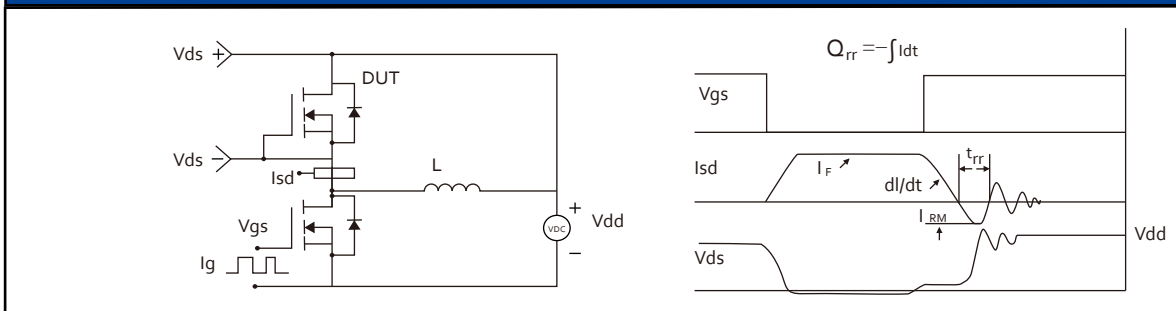
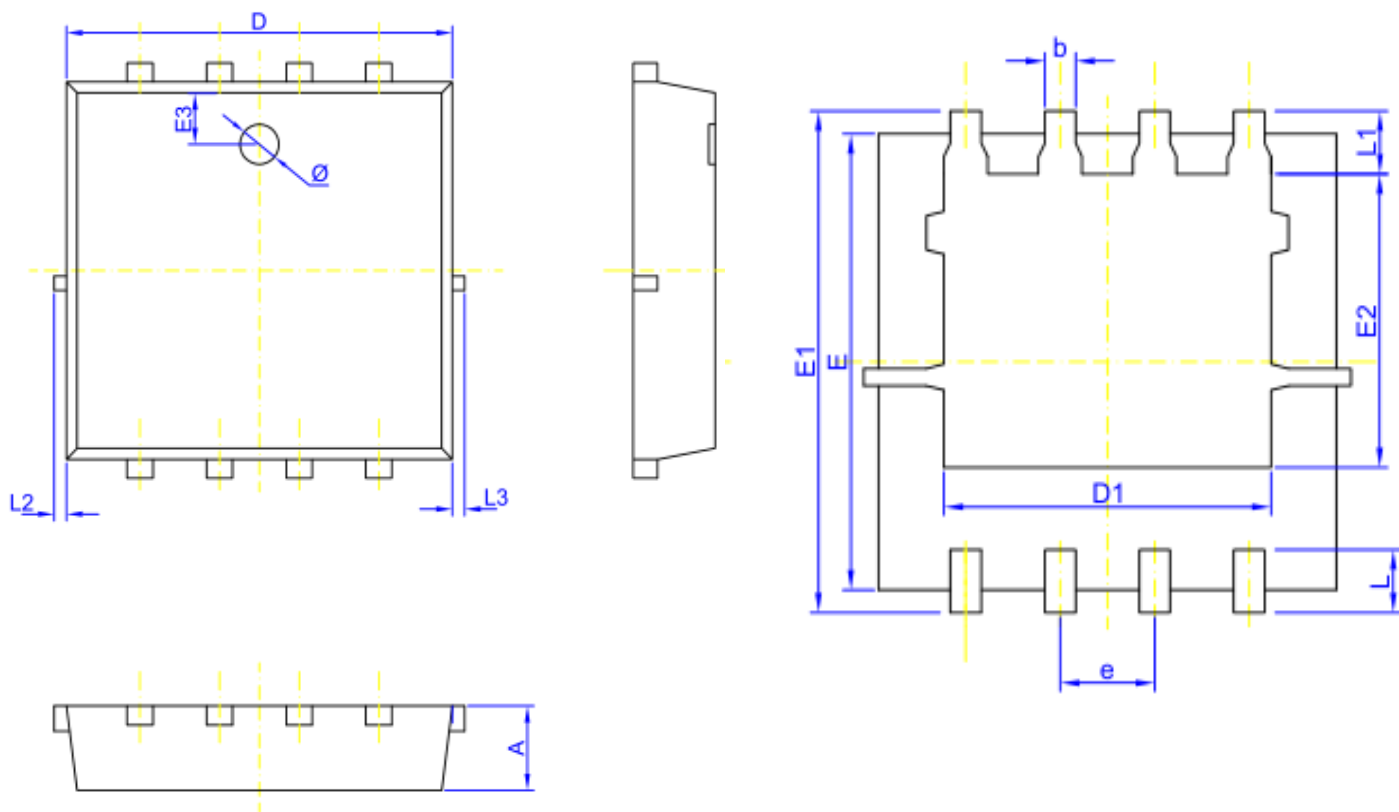


Fig.20 Diode Recovery Test Circuit & Waveforms



## 8. Package Dimensions

### PDFN5\*6 Package



Symbol	Dimensions In Millimeters		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
D	4.950	5.050	5.150
D1	3.850	4.050	4.250
E	5.750	5.850	5.950
E1	5.950	6.150	6.350
E2	3.300	3.500	3.700
E3	0.900	1.100	1.300
b	0.250	0.300	0.350
e	1.220	1.270	1.320
L	0.585	0.685	0.785
L1	0.525	0.625	0.725
∅	1.000	1.200	1.400
L2	0~0.100		
L3	0~0.100		

## 9. Record of Document amendment

产品名称：LN018N040G  
版权说明：镭诺电子（宁波）有限公司  
联系电话：4008887385

文档类型：产品手册  
公司主页：[www.leinuosemi.com](http://www.leinuosemi.com)

版本：02

修改记录：

- 1.初版发行
- 2.修改Fig.13不同温度下内阻值的相对变化量，采用归一化物理量变化单位值（P.U.）
- 3.修正 $R_{\theta JC}$ 数据