

## -100V P-Channel Enhancement Mode MOSFET

### 1. Product Information

#### 1.1 Features

- ◇ Advanced TRENCH cell design
- ◇ Low Gate Charge
- ◇ Low On-Resistance
- ◇ RoHS and Halogen-Free Compliant
- ◇ 100%  $\Delta V_{DS}$  & UIS & Rg Tested

#### 1.2 Applications

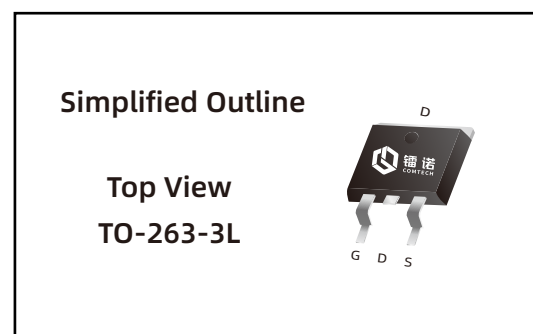
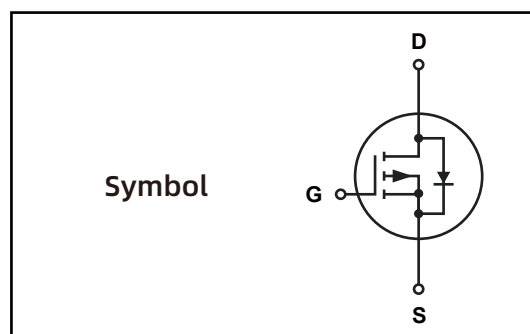
- ◇ DC-DC Converter
- ◇ Drones
- ◇ Motor drivers
- ◇ Light electric vehicles

#### 1.3 Quick reference

- ◇  $BV \cong -100\text{ V}$
- ◇  $P_{\text{tot}} \cong 183\text{ W}$
- ◇  $I_D \cong -57\text{ A}$
- ◇  $R_{DS(\text{ON})} \cong 32\text{ m}\Omega @ V_{GS} = -10\text{ V}$
- ◇  $R_{DS(\text{ON})} \cong 34\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$



### 2. Pin Description



### 3.Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit	Note
$V_{DS}$	Drain-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	-100	V	-
$V_{GS}$	Gate-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	$\pm 20$	V	-
$I_D^*$	Drain Current ( DC )	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = -10\text{ V}$	-	-57	A	Fig.2
		$T_C = 100\text{ }^\circ\text{C}, V_{GS} = -10\text{ V}$	-	-36	A	
$I_{DM}^{**},^{***}$	Drain Current ( Pulsed )	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = -10\text{ V}$	-	-85	A	-
$P_{tot}$	Drain power dissipation	$T_C = 25\text{ }^\circ\text{C}$	-	183	W	Fig.1
		$T_C = 100\text{ }^\circ\text{C}$	-	73	W	
$T_{stg}$	Storage Temperature		-55	150	$^\circ\text{C}$	-
$T_J$	Junction Temperature		-	150	$^\circ\text{C}$	-
$I_S$	Continuous-Source Current	$T_C = 25\text{ }^\circ\text{C}$	-	-57	A	-
$E_{AS}^*$	Single Pulsed Avalanche Energy	$V_{DD} = -100\text{ V}, L = 0.1\text{ mH}$	-	500	mJ	Fig.19

### 4.Thermal Characteristics

$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient	-	26	$^\circ\text{C/W}$	Fig.16
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case	-	0.68		

Notes :

\* Surface Mounted on 1 in<sup>2</sup> pad area,  $t \leq 10\text{ sec}$

\*\* Pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$

\*\*\* limited by bonding wire

### 5.Marking Information

Product Name	Package	Reel size	Tape width	Quantity	Note
LN270P100K	TO-263-3L	330mm	24mm	800	

Note: COMTECH defines " Green " as lead-free ( RoHS compliant ) and halogen free ( Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C )

## 6. Electrical Characteristics ( $T_A=25^\circ$ Unless Otherwise Noted )

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
<b>Static Characteristics</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = -250\ \mu\text{A}$	-100	-	-	V	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = -250\ \mu\text{A}$	-1	-	-3	V	
$I_{DSS}$	Drain Leakage Current	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$	
$I_{GSS}$	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA	
$R_{DS(on)}^a$	On-State Resistance	$V_{GS} = -10\text{ V}, I_{DS} = -30\text{ A}$	-	30	32	m $\Omega$	Fig.8
		$V_{GS} = -4.5\text{ V}, I_{DS} = -20\text{ A}$	-	32	34		
<b>Diode Characteristics</b>							
$V_{SD}^a$	Diode Forward Voltage	$I_{SD} = -30\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V	Fig.7
$t_{rr}$	Reverse Recovery Time	$I_{DS} = -30\text{ A}, V_{GS} = 0\text{ V}$	-	38	-	nS	Fig.20
$Q_{rr}$	Reverse Recovery Charge	$dI_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	210	-	nC	
<b>Dynamic Characteristics<sup>b</sup></b>							
$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = -50\text{ V}$ Frequency = 1 MHz	-	8159	-	pF	Fig.10
$C_{OSS}$	Output Capacitance		-	192	-		
$C_{rSS}$	Reverse Transfer Capacitance		-	155	-		
$R_G$	Gate Resistance	F= 1 MHz	-	3.1	-	$\Omega$	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = -50\text{ V}, V_{GS} = 10\text{ V},$ $R_G=2.7\ \Omega, R_L = 20\ \mu\text{H},$ $I_{DS} = -30\text{ A}$	-	24	-	nS	Fig.18
$t_r$	Turn-on Rise Time		-	105	-		
$t_d(off)$	Turn-off Delay Time		-	132	-		
$t_f$	Turn-off Fall Time		-	42	-		
$dv/dt$	Peak Diode Recovery		-	0.381	-		
$di/dt$	Peak Diode Recovery	-	399	-	A/us		
<b>Gate Charge Characteristics<sup>b</sup></b>							
$Q_g$	Total Gate Charge	$V_{DS} = -50\text{ V}, V_{GS} = -10\text{ V},$ $I_{DS} = -30\text{ A}$	-	120	-	nC	Fig.17
$Q_{gs}$	Gate-Source Charge		-	51	-		
$Q_{gd}$	Gate-Drain Charge		-	8	-		
$V_{plateau}$	Gate plateau voltage		-	3.5	-	V	Fig.9

Notes :

a : Pulse test ; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$

b : Guaranteed by design, not subject to production testing

## 7. Typical Characteristics

Fig.1 Power Capability

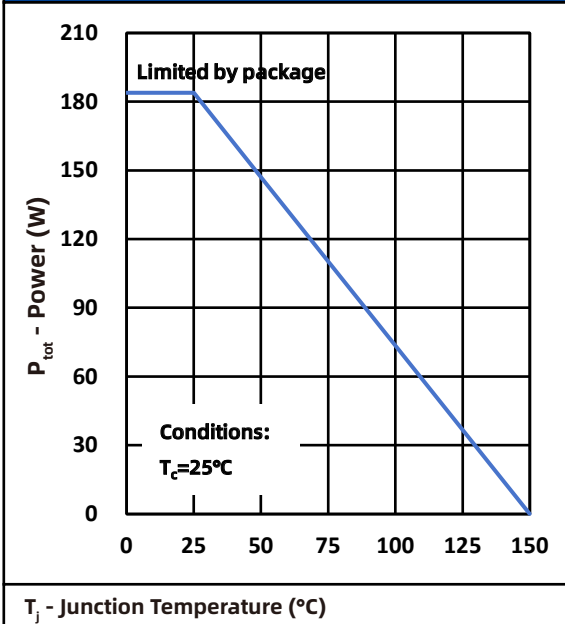


Fig.2 Current Capability

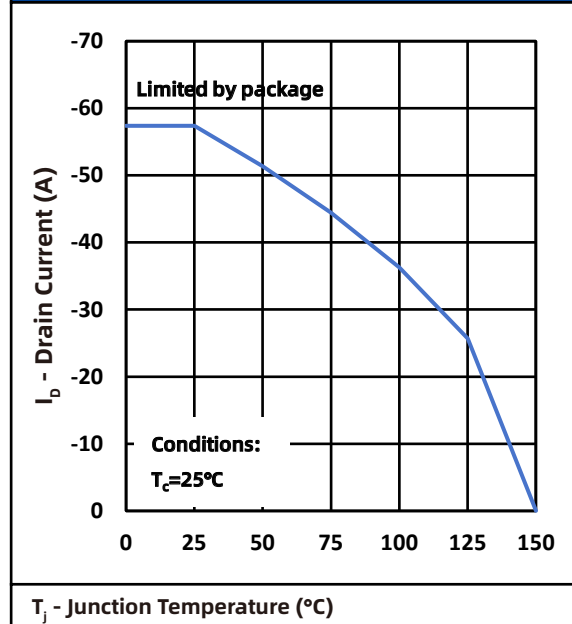


Fig.3 Output Characteristics@ $T_j$  -55°C

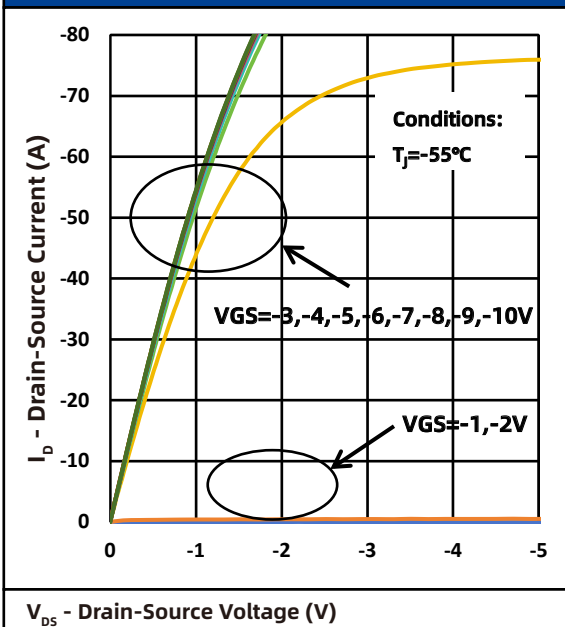
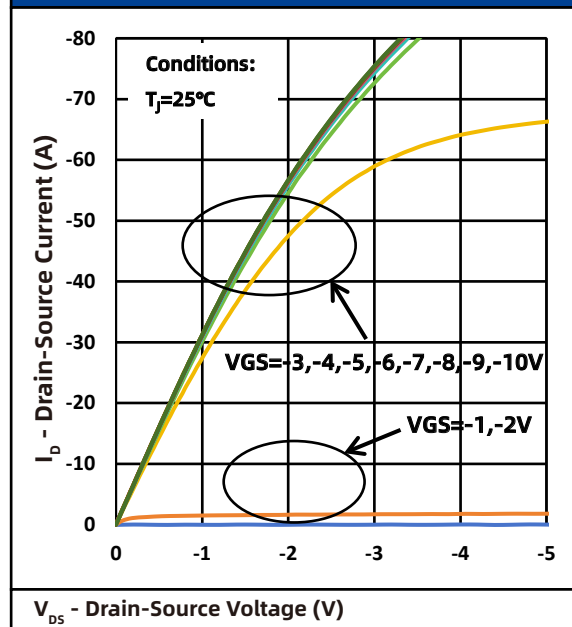
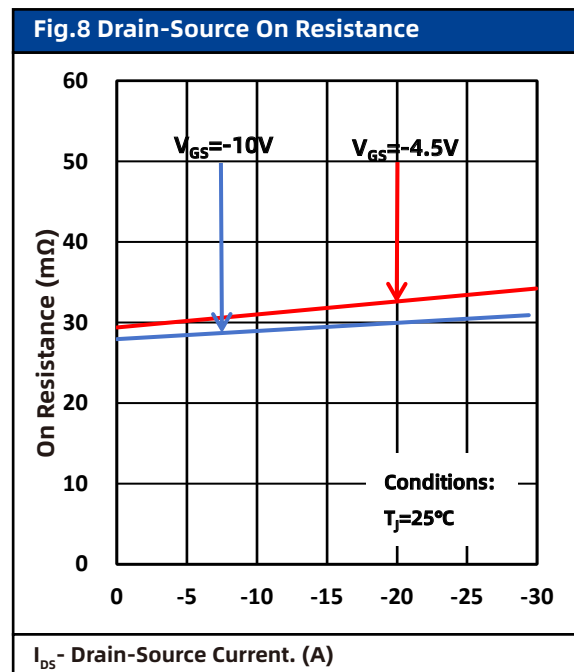
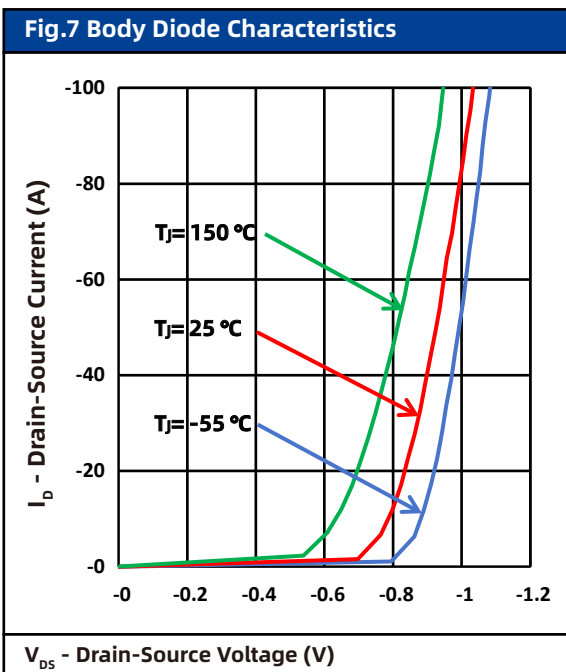
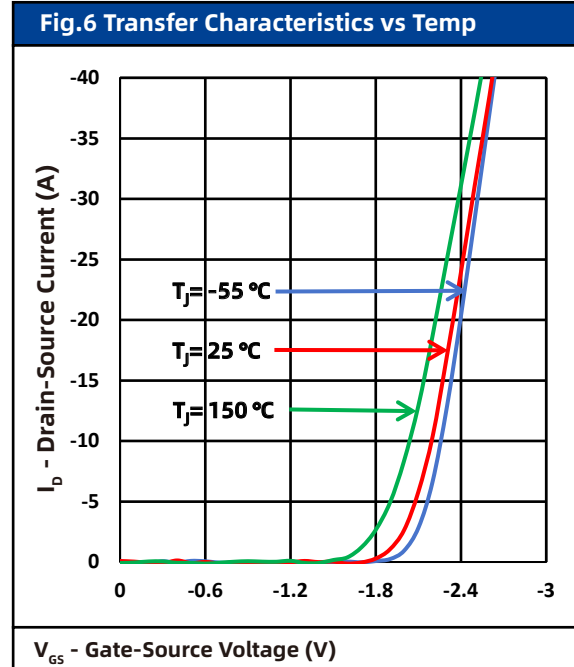
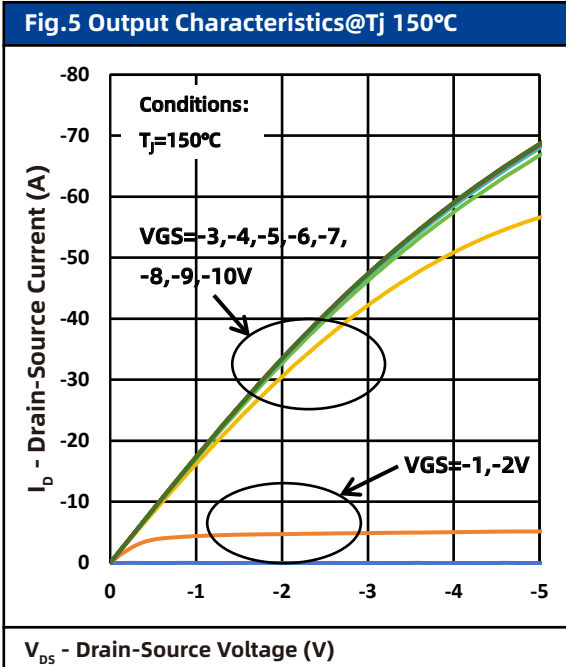


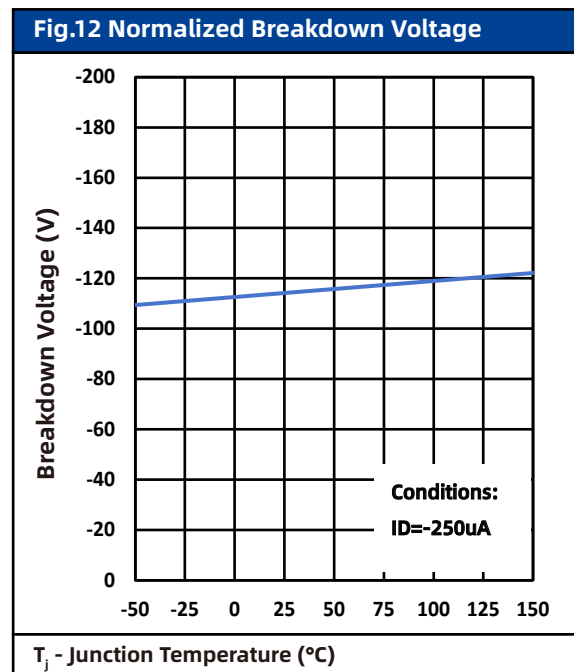
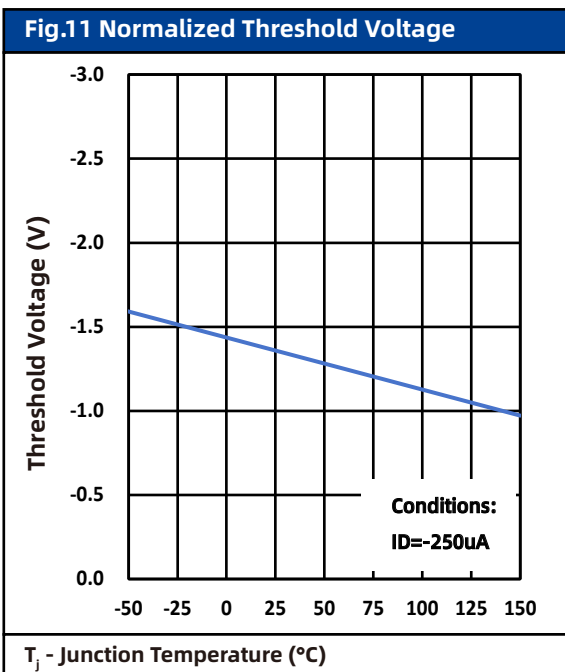
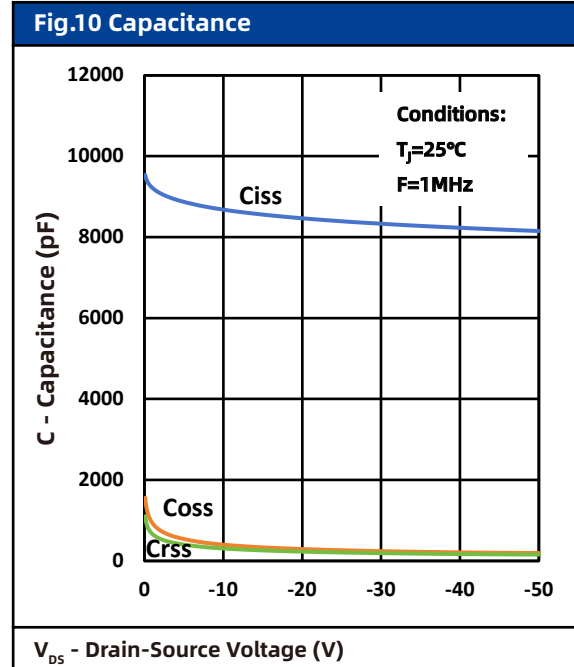
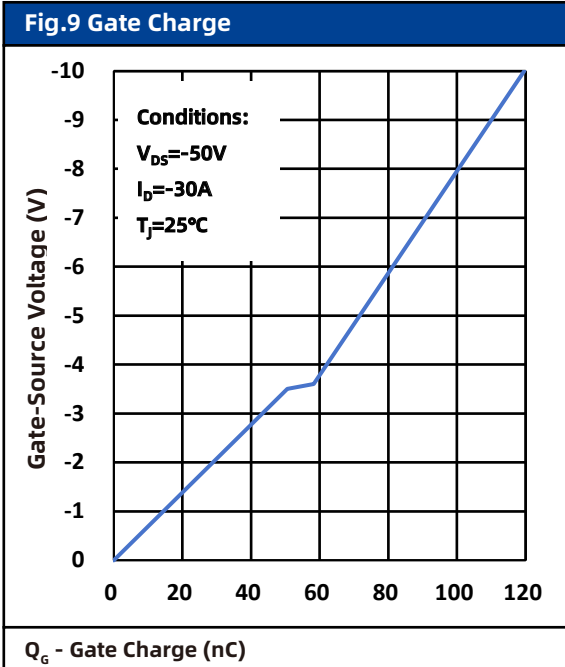
Fig.4 Output Characteristics@ $T_j$  25°C



## 7. Typical Characteristics



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Fig.13 Normalized On Resistance

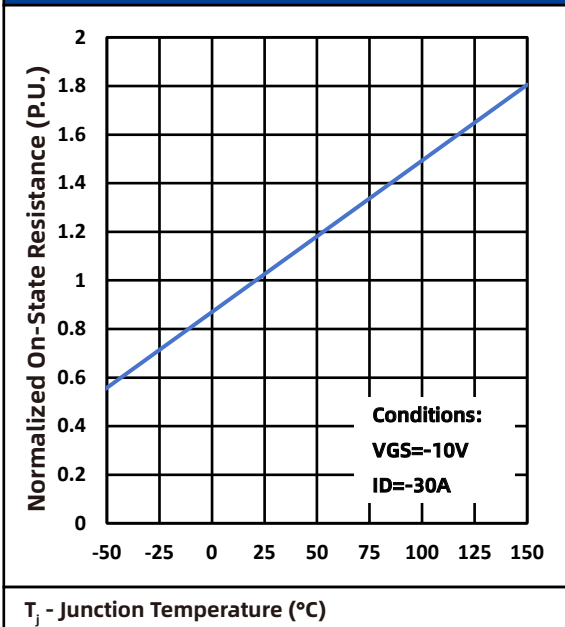


Fig.14 Switching Energy vs I<sub>D</sub>

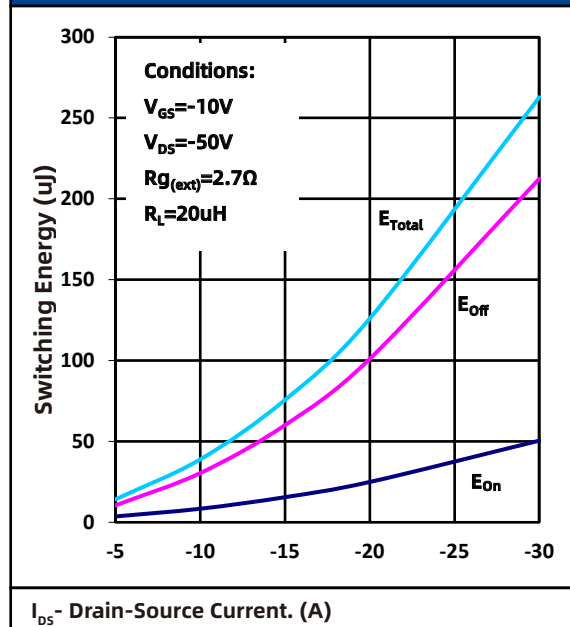


Fig.15 Safe Operating Area

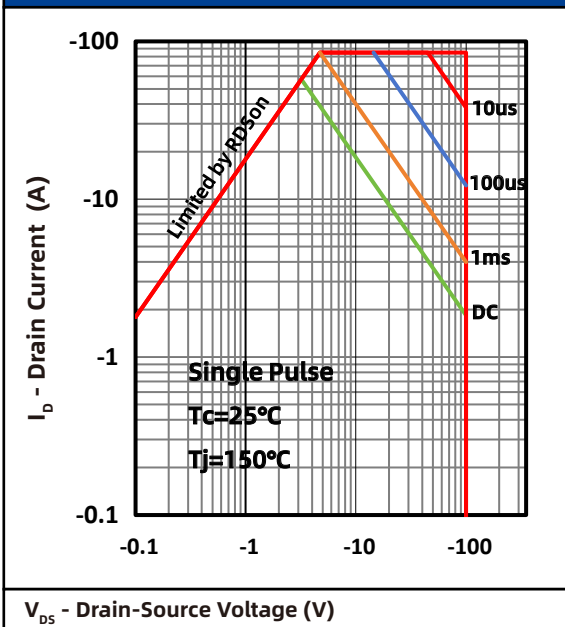
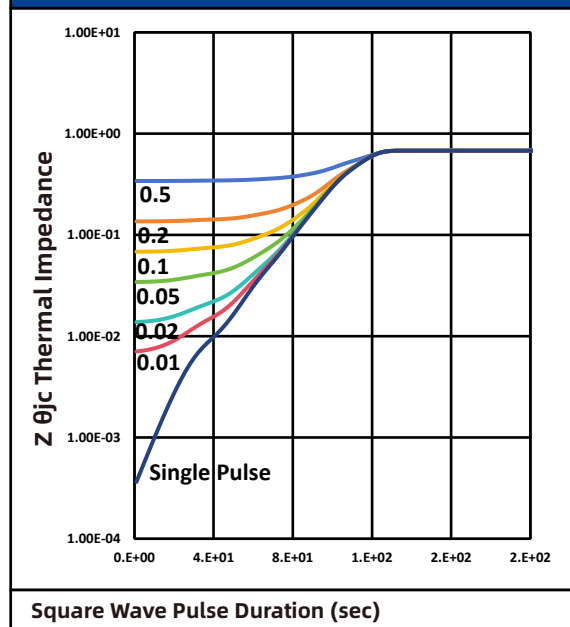


Fig.16 Transient Thermal Impedance



## 7. Typical Characteristics

Fig.17 Gate Charge Test Circuit & Waveform

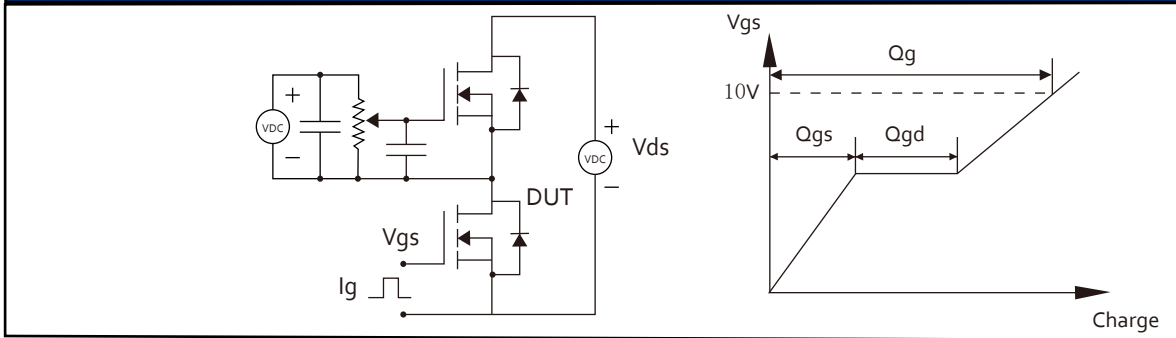


Fig.18 Resistive Switching Test Circuit & Waveforms

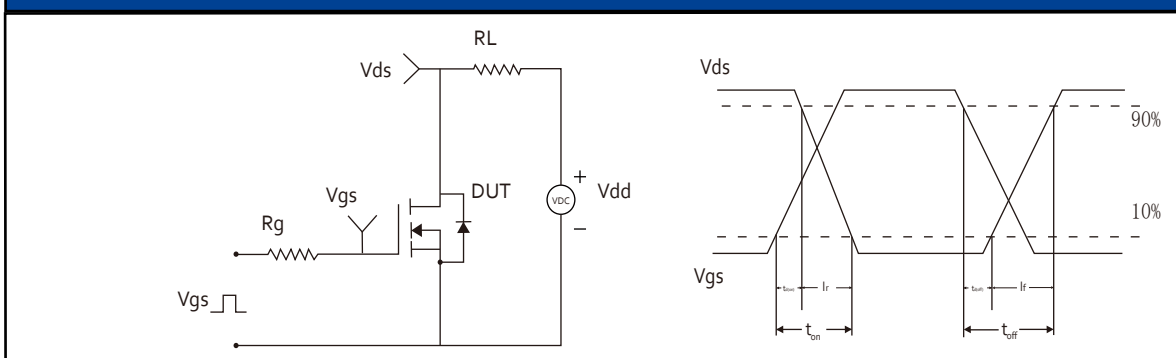


Fig.19 Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

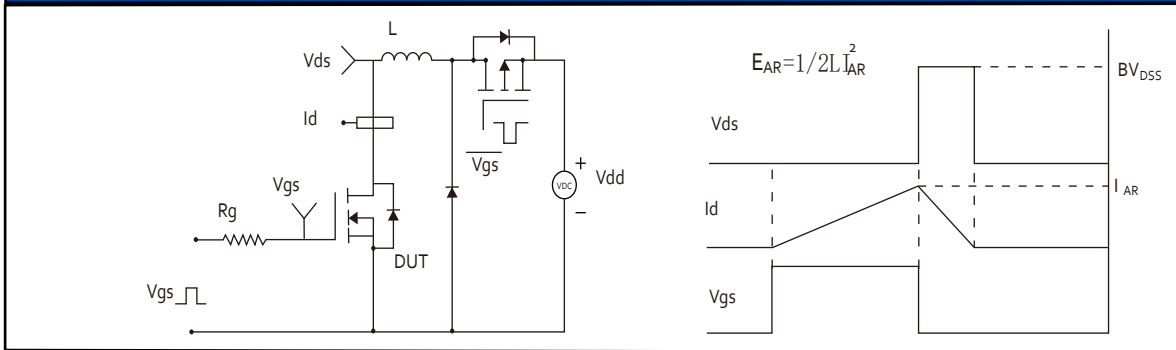
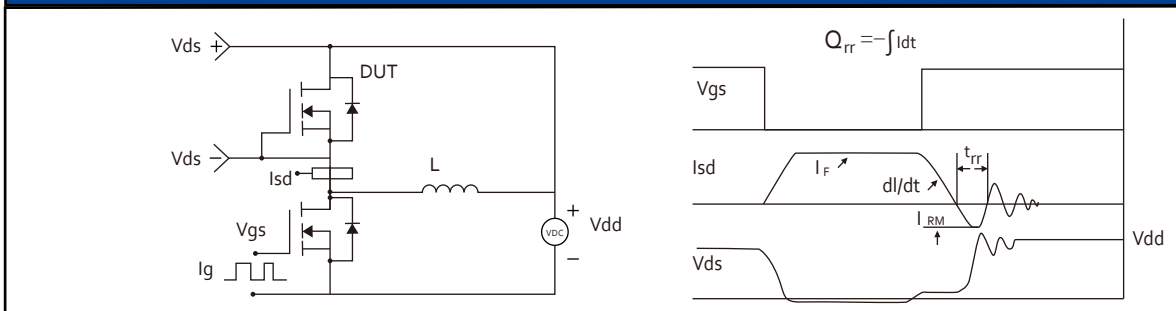
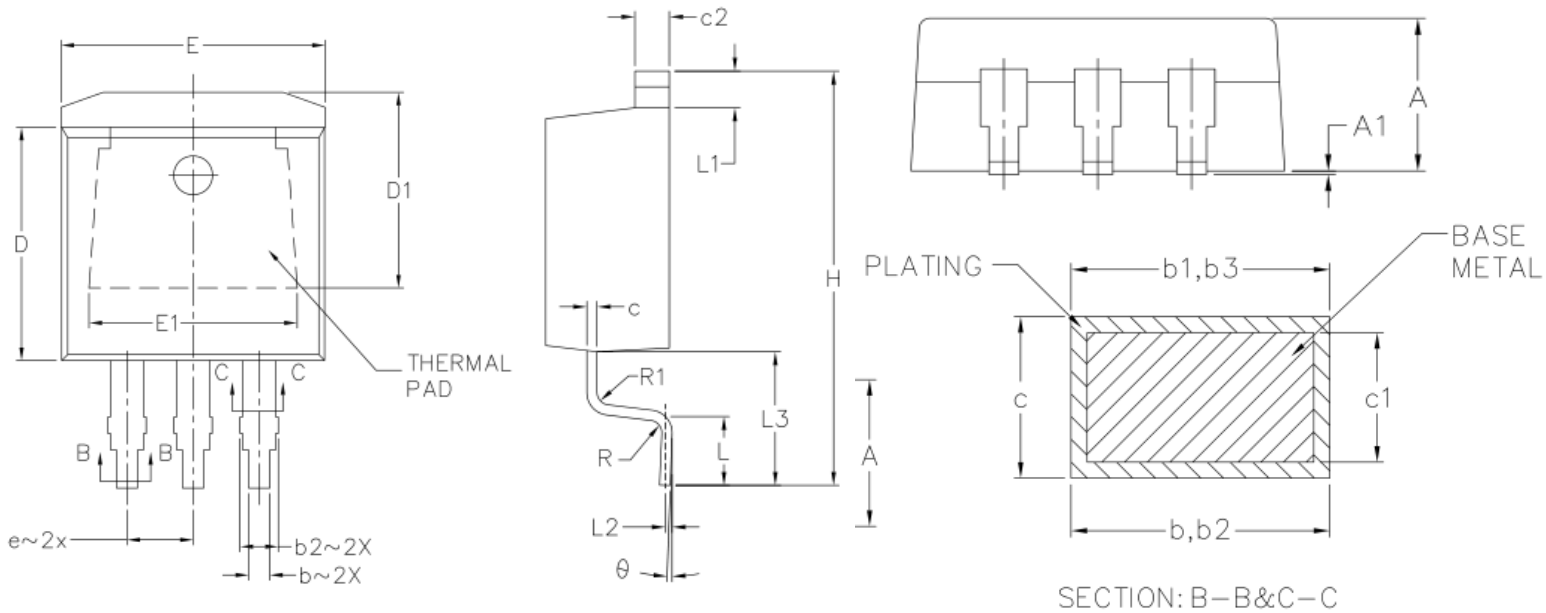


Fig.20 Diode Recovery Test Circuit & Waveforms



## 8. Package Dimensions

### TO-263-3L Package



Symbol	Dimensions In Millimeters		
	MIN.	NOM.	MAX.
A	4.064	4.445	4.826
A1	0.000	0.127	0.254
b	0.508	0.749	0.991
b1	0.508	0.698	0.889
b2	1.143	1.460	1.778
b3	1.143	1.435	1.727
c	0.381	0.559	0.737
c1	0.381	0.482	0.584
c2	1.143	1.397	1.651
D	8.382	9.017	9.652
D1	6.858	-	-
E	9.652	10.160	10.668
E1	6.223	-	-
e		2.540 BSC.	
H	14.605	15.240	15.875
L	1.778	2.286	2.794
L1	-	-	1.676
L2		0.254 BSC.	
L3	4.780	5.030	5.280
R		0.460 TYP	
R1		0.460 TYP	
θ	0°	4°	8°

## 9. Record of Document amendment

产品名称：LN270P100K  
版权说明：镭诺电子（宁波）有限公司  
联系电话：4008887385

文档类型：产品手册  
公司主页：[www.leinuosemi.com](http://www.leinuosemi.com)

版本：01  
修改记录：  
1.初版发行