

40V N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ◇ Advanced SGT cell design
- ◇ Low Gate Charge
- ◇ Low On-Resistance
- ◇ RoHS and Halogen-Free Compliant
- ◇ 100% ΔV_{DS} & UIS & Rg Tested

1.2 Applications

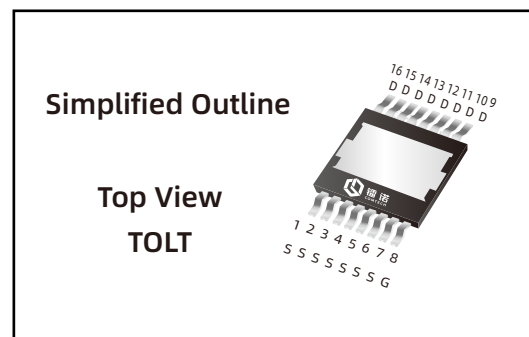
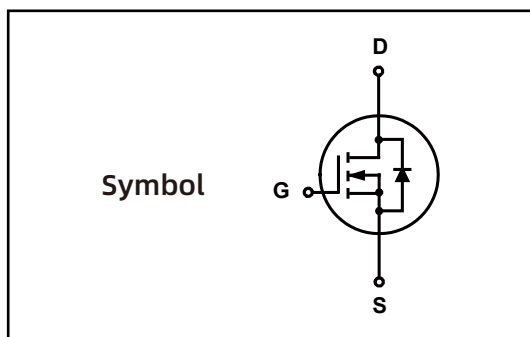
- ◇ DC-DC Converter
- ◇ Drones
- ◇ Motor drivers
- ◇ Light electric vehicles

1.3 Quick reference

- ◇ $BV \cong 40\text{ V}$
- ◇ $P_{\text{tot}} \cong 517\text{ W}$
- ◇ I_D (Silicon Limited) $\cong 657\text{ A}$
- ◇ I_D (Package Limited) $\cong 500\text{ A}$
- ◇ $R_{DS(ON)} \cong 0.85\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- ◇ $R_{DS(ON)} \cong 2.2\text{ m}\Omega @ V_{GS} = 6\text{ V}$



2. Pin Description



3.Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit	Note
V_{DS}	Drain-Source Voltage	$T_c = 25\text{ }^\circ\text{C}$	-	40	V	-
V_{GS}	Gate-Source Voltage	$T_c = 25\text{ }^\circ\text{C}$	-	± 20	V	-
I_D^*	Drain Current (DC) (Silicon Limited)	$T_c = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	657	A	Fig.2
		$T_c = 100\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	464	A	
	Drain Current (DC) (Package Limited)	$T_c = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	500	A	
		$T_c = 100\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	354	A	
$I_{DM}^{**},^{***}$	Drain Current (Pulsed)	$T_c = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	747	A	-
P_{tot}	Drain power dissipation	$T_c = 25\text{ }^\circ\text{C}$	-	517	W	Fig.1
		$T_c = 100\text{ }^\circ\text{C}$	-	258	W	
T_{stg}	Storage Temperature		-55	175	$^\circ\text{C}$	-
T_J	Junction Temperature		-	175	$^\circ\text{C}$	-
I_S	Continuous-Source Current	$T_c = 25\text{ }^\circ\text{C}$	-	500	A	-
E_{AS}^*	Single Pulsed Avalanche Energy	$V_{DD} = 40\text{ V}, L = 0.1\text{ mH}$	-	1248	mJ	Fig.19

4.Thermal Characteristics

$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient	-	21	$^\circ\text{C}/\text{W}$	Fig.16
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case	-	0.29		

Notes :

- * Surface Mounted on 1 in² pad area, $t \leq 10\text{ sec}$
- ** Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- *** limited by bonding wire

5.Marking Information

Product Name	Package	Reel size	Tape width	Quantity	Note
LN006N040LT-H	TOLT	330mm	24mm	1800	

Note: COMTECH defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

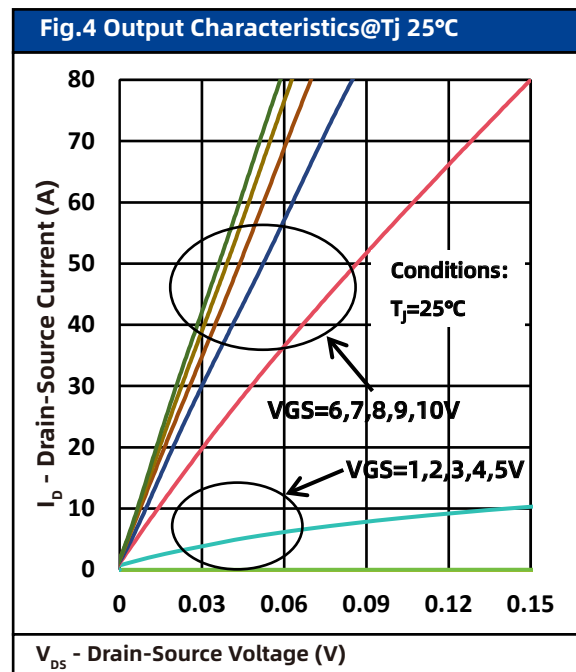
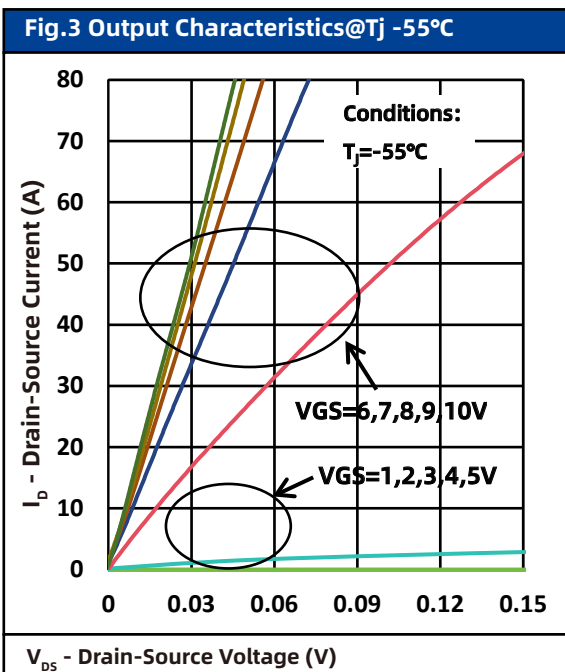
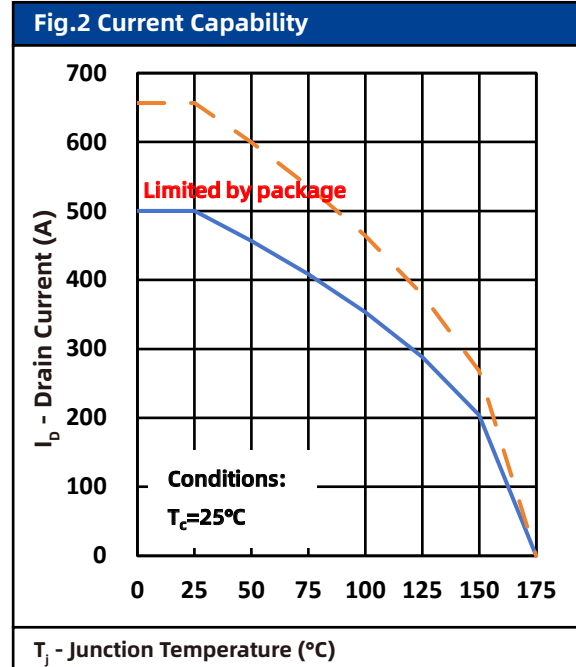
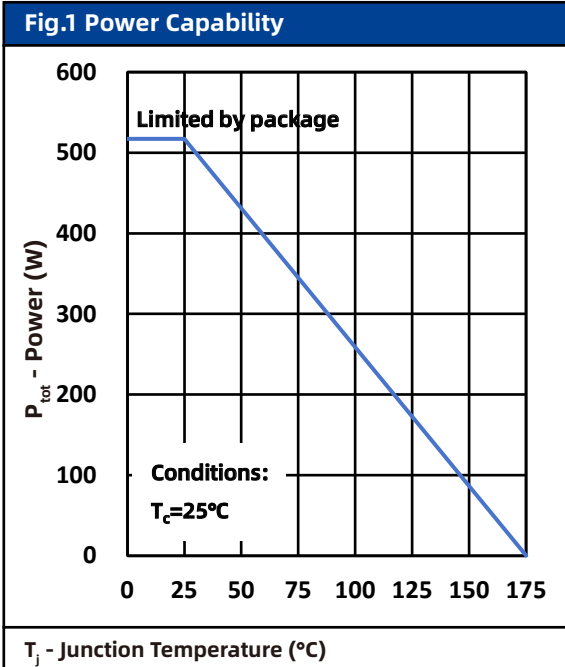
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
Static Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	40	-	-	V	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	2	-	4	V	
I_{DSS}	Drain Leakage Current	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA	
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA	
$R_{DS(on)}^a$	On-State Resistance	$V_{GS} = 10\text{ V}, I_{DS} = 50\text{ A}$	-	0.75	0.85	m Ω	Fig.8
		$V_{GS} = 6\text{ V}, I_{DS} = 30\text{ A}$	-	1.8	2.2		
Diode Characteristics							
V_{SD}^a	Diode Forward Voltage	$I_{SD} = 50\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V	Fig.7
t_{rr}	Reverse Recovery Time	$I_{DS} = 50\text{ A}, V_{GS} = 0\text{ V}$	-	44	-	nS	Fig.20
Q_{rr}	Reverse Recovery Charge	$di_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	83	-	nC	
Dynamic Characteristics^b							
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$ Frequency = 1 MHz	-	10360	-	pF	Fig.10
C_{oss}	Output Capacitance		-	3512	-		
C_{riss}	Reverse Transfer Capacitance		-	357	-		
R_G	Gate Resistance	F= 1 MHz	-	2.8	-	Ω	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V},$ $R_G = 2.7\ \Omega, R_L = 4\ \mu\text{H},$ $I_{DS} = 50\text{ A}$	-	43	-	nS	Fig.18
t_r	Turn-on Rise Time		-	220	-		
$t_d(off)$	Turn-off Delay Time		-	78	-		
t_f	Turn-off Fall Time		-	53	-		
dv/dt	Peak Diode Recovery		-	0.073	-		
di/dt	Peak Diode Recovery	-	260	-	A/us		
Gate Charge Characteristics^b							
Q_g	Total Gate Charge	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V},$ $I_{DS} = 50\text{ A}$	-	138	-	nC	Fig.17
Q_{gs}	Gate-Source Charge		-	33	-		
Q_{gd}	Gate-Drain Charge		-	57	-		
$V_{plateau}$	Gate plateau voltage		-	4.8	-		

Notes :

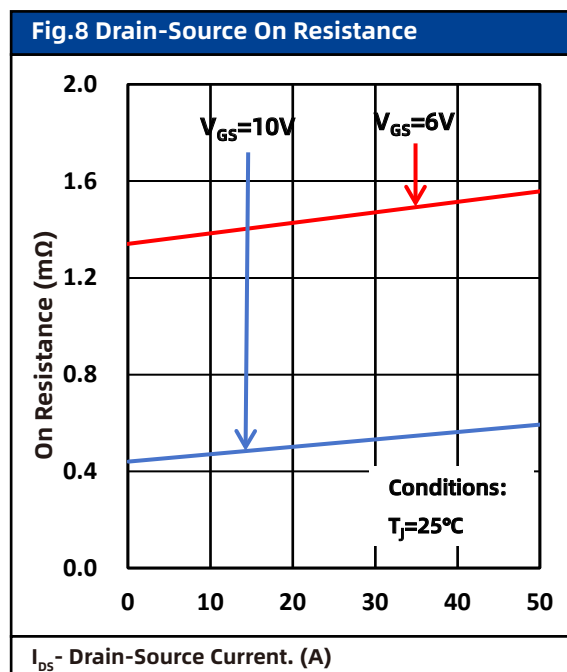
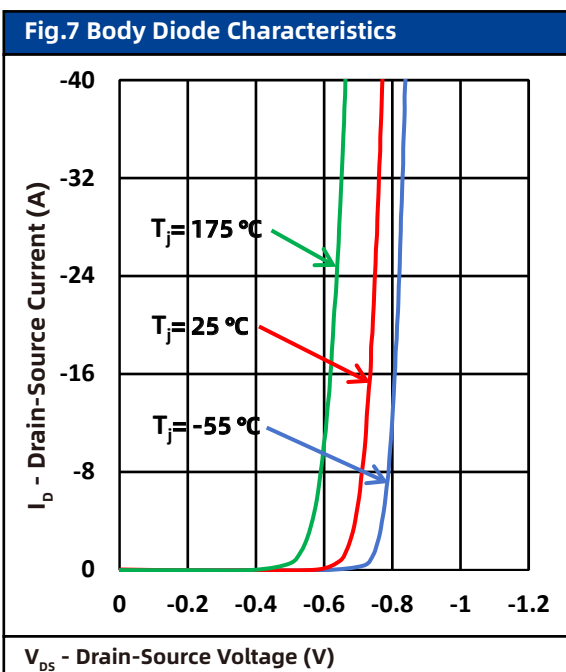
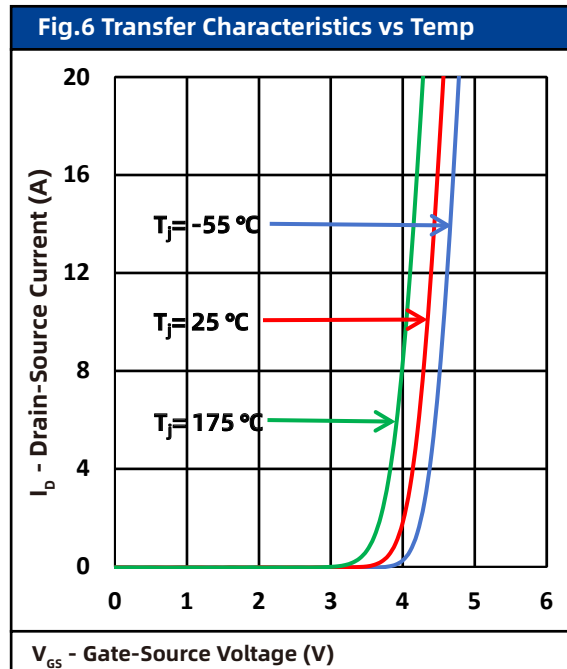
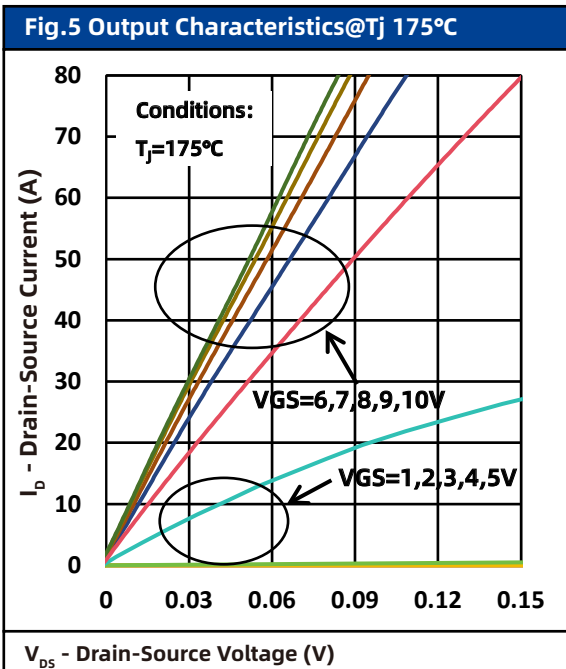
a : Pulse test ; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

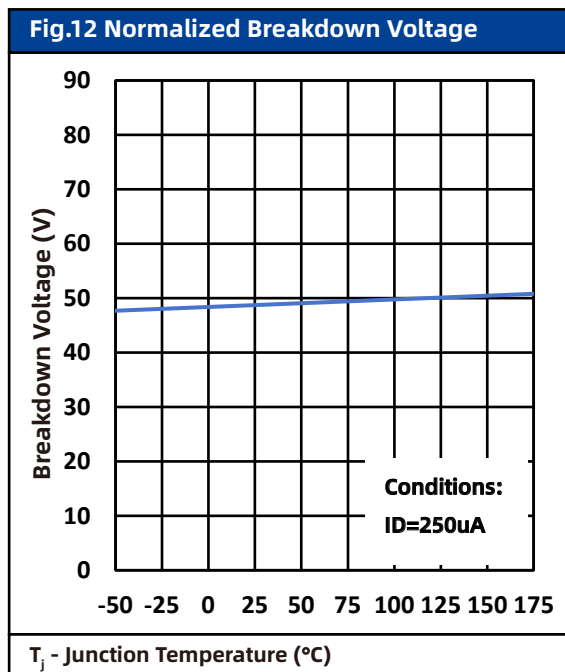
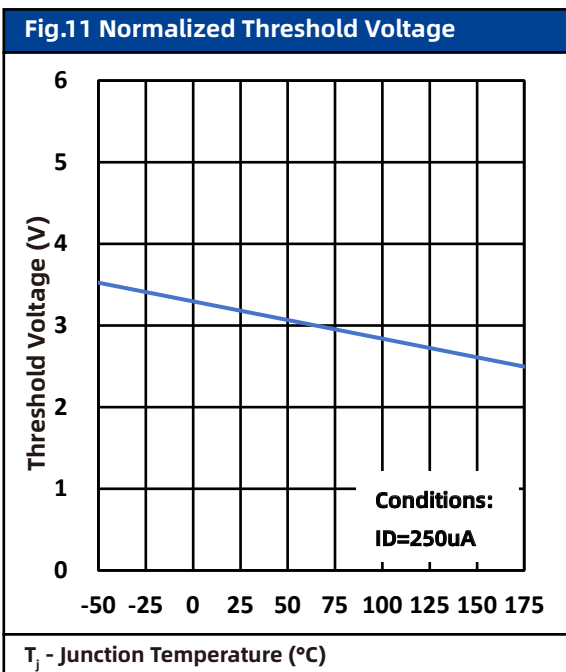
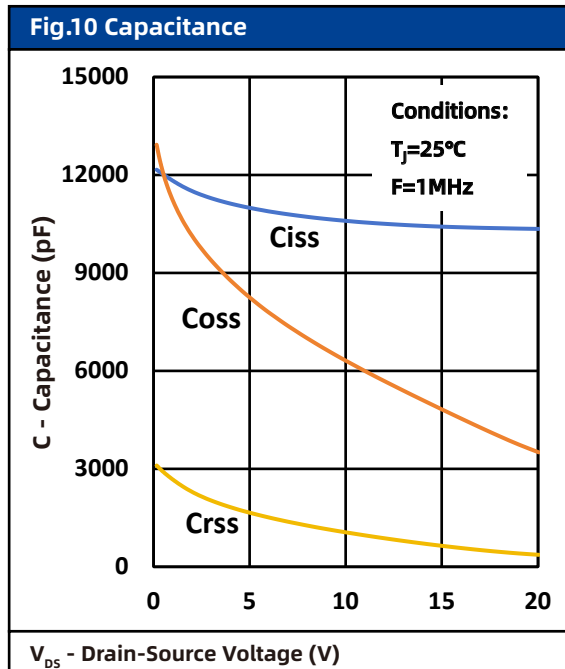
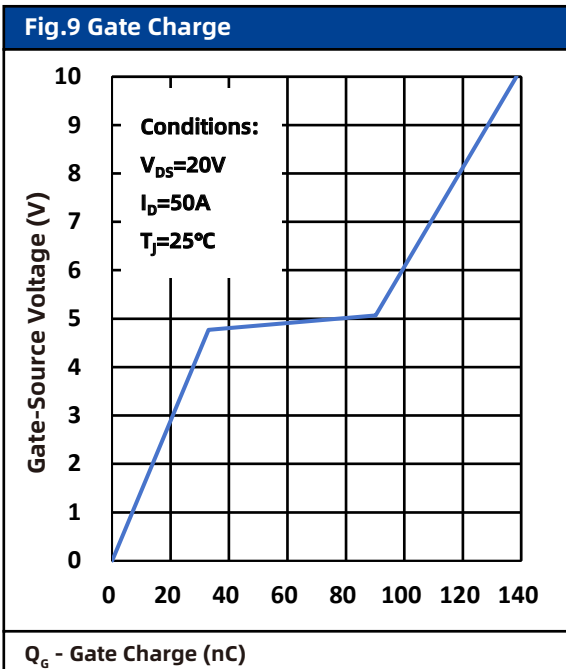
7. Typical Characteristics



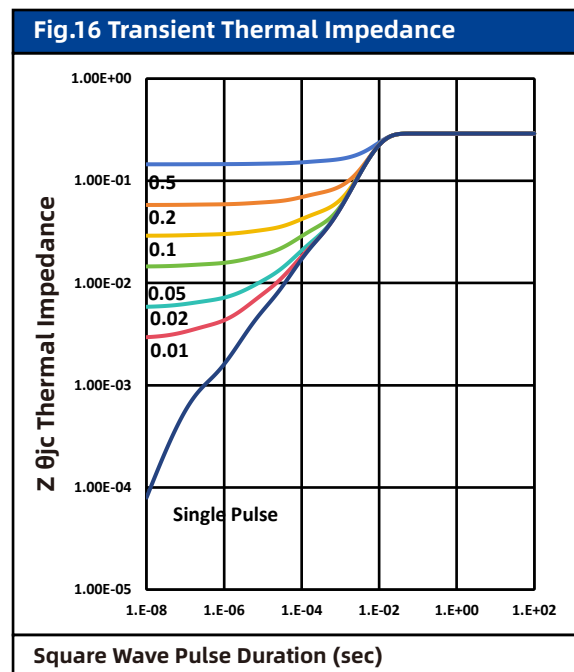
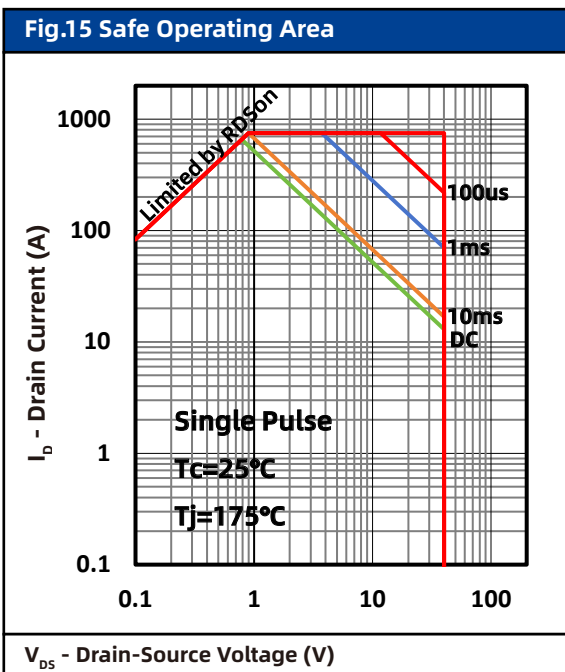
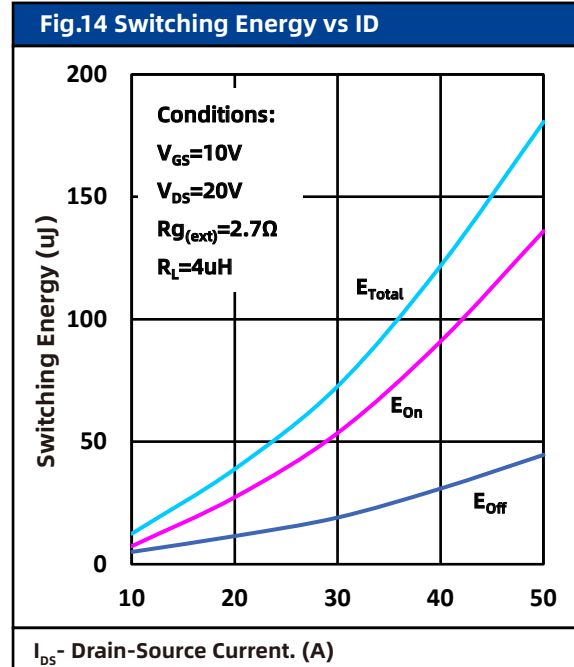
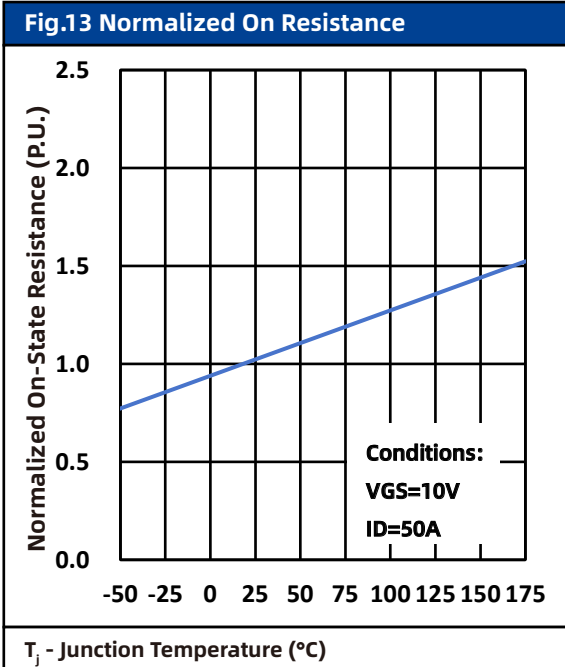
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Fig.17 Gate Charge Test Circuit & Waveform

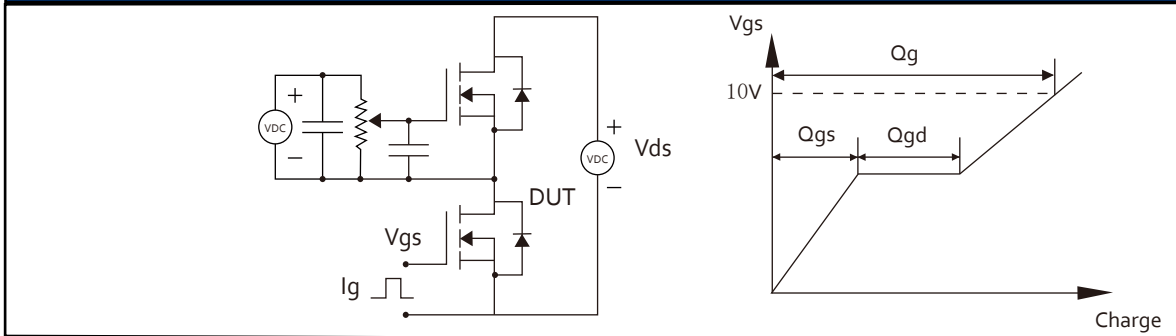


Fig.18 Resistive Switching Test Circuit & Waveforms

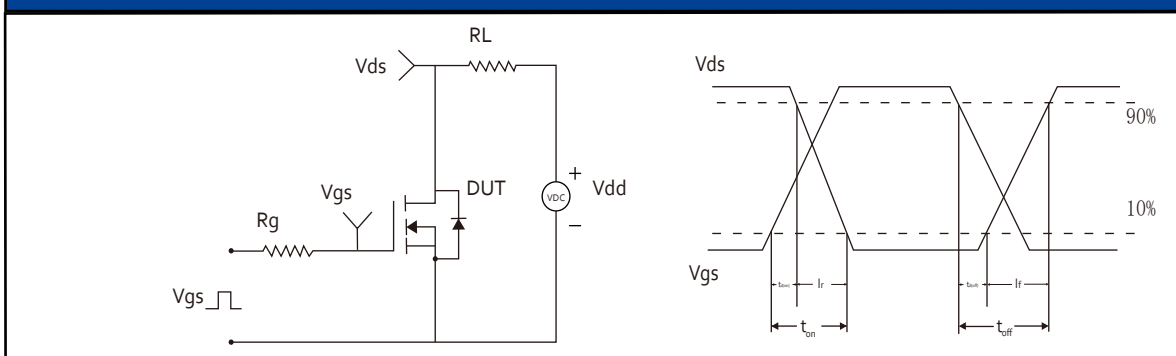


Fig.19 Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

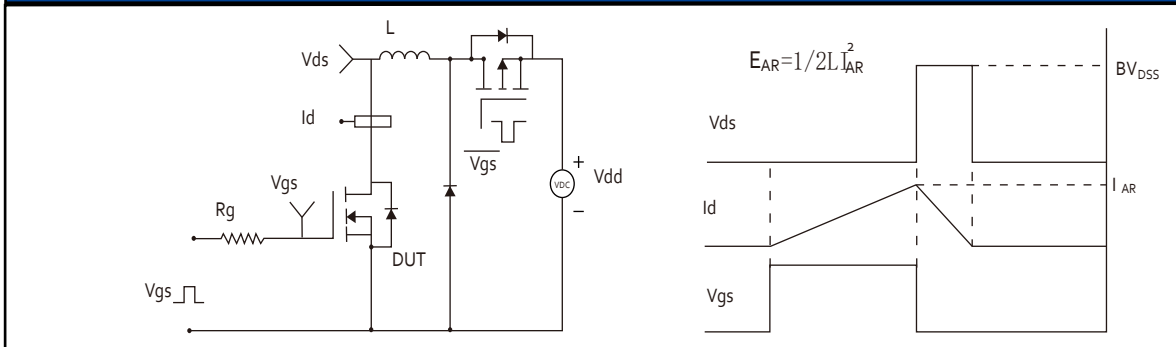
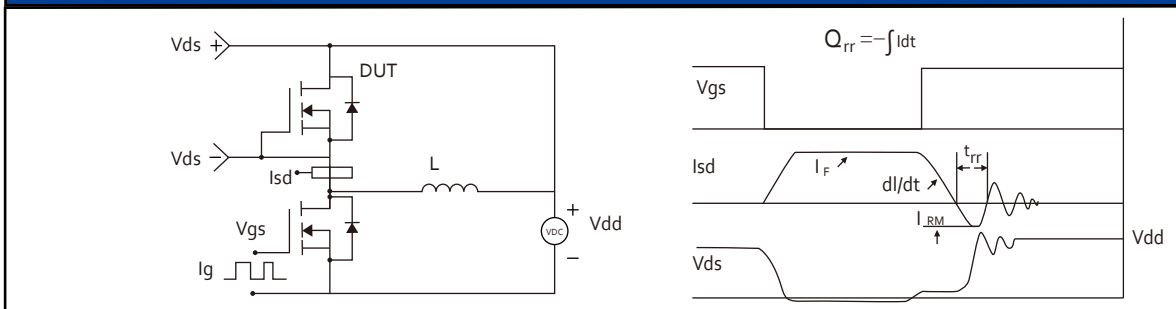
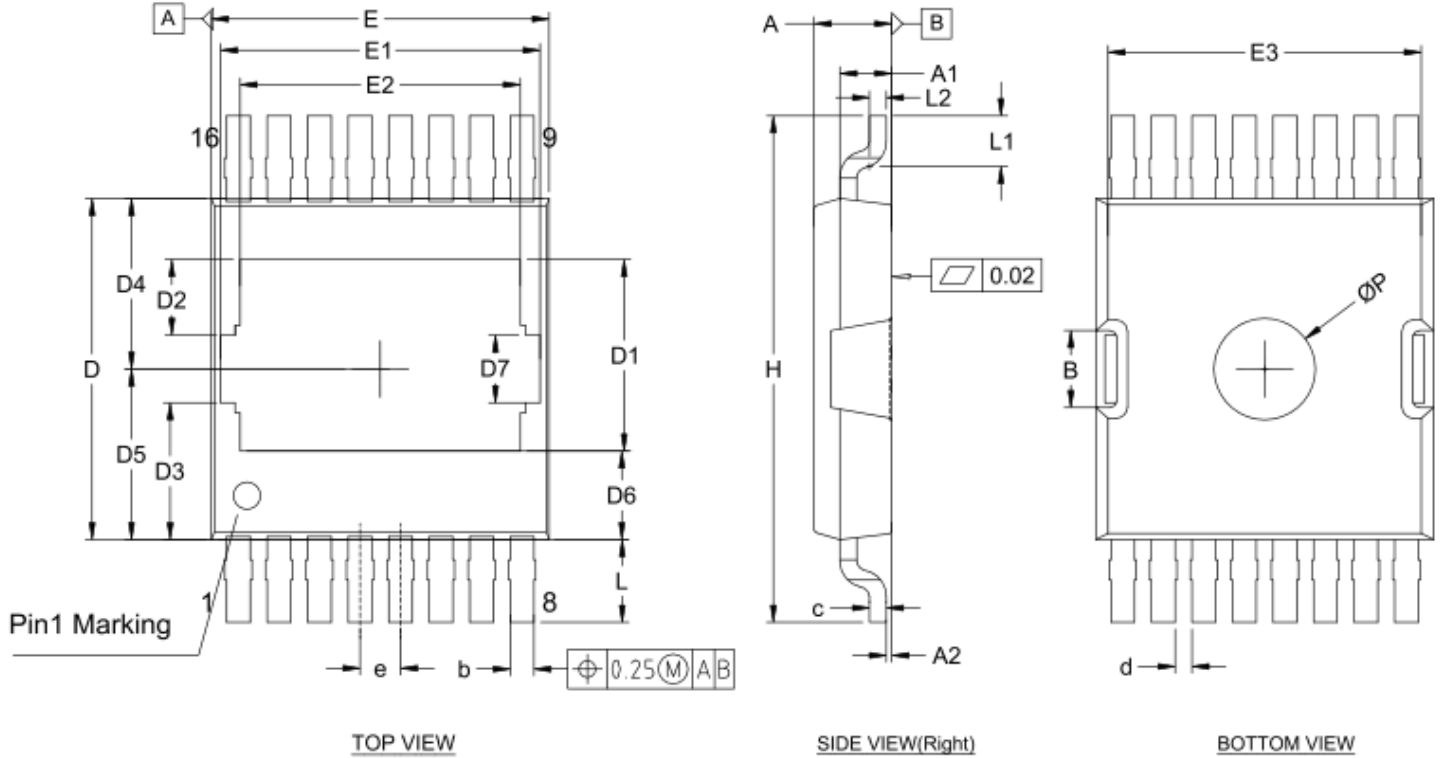


Fig.20 Diode Recovery Test Circuit & Waveforms



8. Package Dimensions

TOLT Package



Symbol	Dimensions In Millimeters		
	MIN.	NOM.	MAX.
A	2.250	2.300	2.350
A1	1.440	1.540	1.640
A2	0.010	-	0.160
b	0.600	0.700	0.800
c	0.400	0.500	0.600
d	0.400	0.500	0.600
e			
D	10.000	10.100	10.300
D1	5.470	5.670	5.870
D2	2.040	2.240	2.440
D3		4.050 REF.	
D4		5.050 REF.	
D5		5.050 REF.	
D6		2.620 REF.	
D7		2.000 REF.	
E	9.700	10.000	10.100
E1		9.460 REF.	
E2	8.100	8.300	8.500
E3	9.070	9.270	9.470
H	14.800	15.000	15.200
L	2.250	2.450	2.650
L1	1.350	1.500	1.650
L2		0.500 BSC.	
ϕP	2.90	3.000	3.100
B	2.180	2.280	2.380

9. Record of Document amendment

产品名称：LN006N040LT-H
版权说明：镭诺电子（宁波）有限公司
联系电话：4008887385

文档类型：产品手册
公司主页：www.leinuosemi.com

版本：01
修改记录：
1.初版发行