

40V N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ◇ Advanced SGT cell design
- ◇ Low Gate Charge
- ◇ Low On-Resistance
- ◇ RoHS and Halogen-Free Compliant
- ◇ 100% ΔV_{DS} & UIS & Rg Tested

1.2 Applications

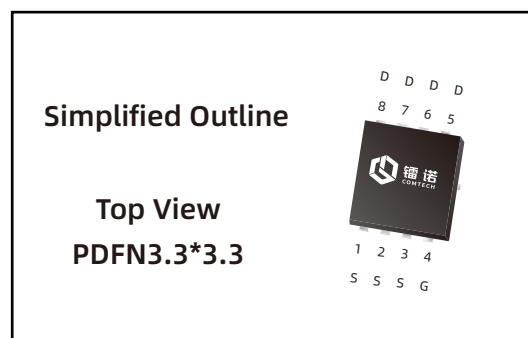
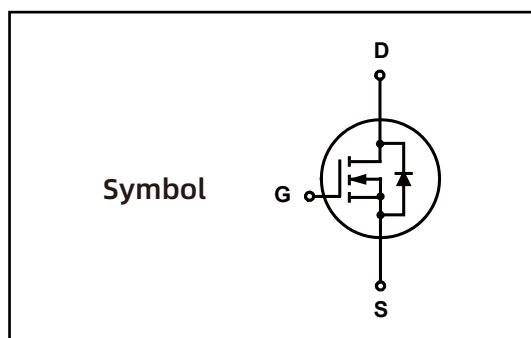
- ◇ DC-DC Converter
- ◇ Drones
- ◇ Motor drivers
- ◇ Light electric vehicles

1.3 Quick reference

- ◇ $BV \cong 40\text{ V}$
- ◇ $P_{\text{tot}} \cong 115\text{ W}$
- ◇ $I_D \cong 196\text{ A}$
- ◇ $R_{DS(ON)} \cong 2.0\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- ◇ $R_{DS(ON)} \cong 3.2\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$



2. Pin Description



3.Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit	Note
V_{DS}	Drain-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	40	V	-
V_{GS}	Gate-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	± 20	V	-
I_D^*	Drain Current (DC)	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	196	A	Fig.2
		$T_C = 100\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	139	A	
$I_{DM}^{**},^{***}$	Drain Current (Pulsed)	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	404	A	-
P_{tot}	Drain power dissipation	$T_C = 25\text{ }^\circ\text{C}$	-	115	W	Fig.1
		$T_C = 100\text{ }^\circ\text{C}$	-	57	W	
T_{stg}	Storage Temperature		-55	175	$^\circ\text{C}$	-
T_J	Junction Temperature		-	175	$^\circ\text{C}$	-
I_S	Continuous-Source Current	$T_C = 25\text{ }^\circ\text{C}$	-	196	A	-
E_{AS}^*	Single Pulsed Avalanche Energy	$V_{DD} = 40\text{ V}, L = 0.1\text{ mH}$	-	171	mJ	Fig.19

4.Thermal Characteristics

$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient	-	36	$^\circ\text{C/W}$	Fig.16
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case	-	1.3		

Notes :

* Surface Mounted on 1 in² pad area, $t \leq 10\text{ sec}$

** Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

*** limited by bonding wire

5.Marking Information

Product Name	Package	Reel size	Tape width	Quantity	Note
LN018N040Q	PDFN3.3*3.3	330mm	12mm	5000	

Note: COMTECH defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

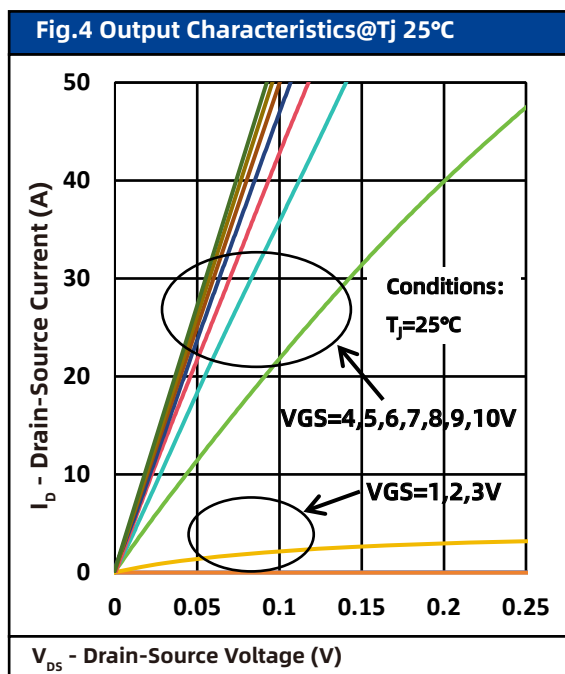
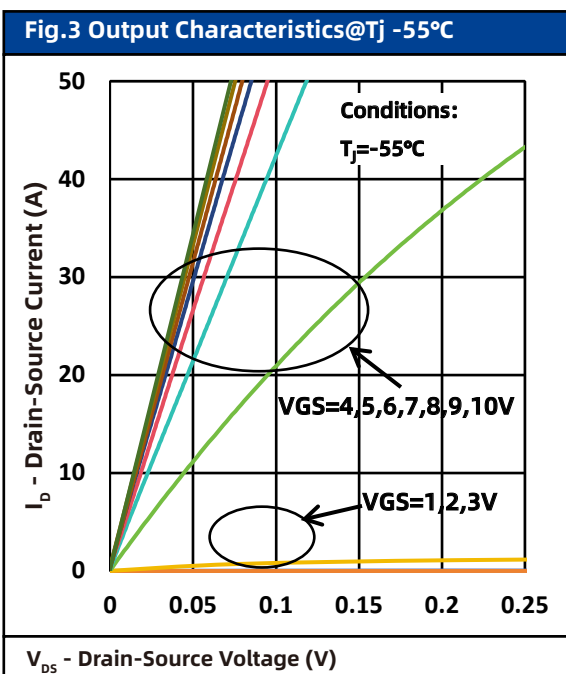
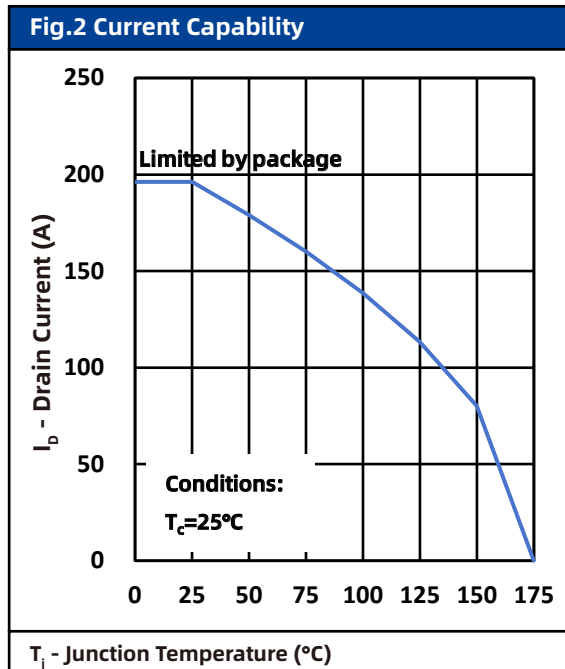
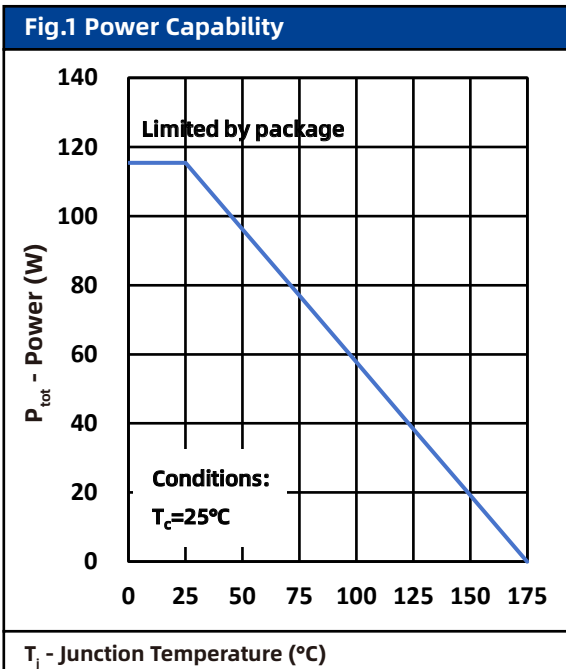
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
Static Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	40	-	-	V	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	1	-	3	V	
I_{DSS}	Drain Leakage Current	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA	
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA	
$R_{DS(on)}^a$	On-State Resistance	$V_{GS} = 10\text{ V}, I_{DS} = 30\text{ A}$	-	1.7	2.0	m Ω	Fig.8
		$V_{GS} = 4.5\text{ V}, I_{DS} = 20\text{ A}$	-	2.7	3.2		
Diode Characteristics							
V_{SD}^a	Diode Forward Voltage	$I_{SD} = 30\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V	Fig.7
t_{rr}	Reverse Recovery Time	$I_{DS} = 30\text{ A}, V_{GS} = 0\text{ V}$	-	27	-	nS	Fig.20
Q_{rr}	Reverse Recovery Charge	$dI_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	23	-	nC	
Dynamic Characteristics^b							
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$ Frequency = 1 MHz	-	2537	-	pF	Fig.10
C_{OSS}	Output Capacitance		-	445	-		
C_{rSS}	Reverse Transfer Capacitance		-	417	-		
R_G	Gate Resistance	F= 1 MHz	-	1.6	-	Ω	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V},$ $R_G=2.7\ \Omega, R_L = 10\ \mu\text{H},$ $I_{DS} = 30\text{ A}$	-	24	-	nS	Fig.18
t_r	Turn-on Rise Time		-	133	-		
$t_d(off)$	Turn-off Delay Time		-	46	-		
t_f	Turn-off Fall Time		-	23	-		
dv/dt	Peak Diode Recovery		-	0.121	-		
di/dt	Peak Diode Recovery	-	291	-	A/us		
Gate Charge Characteristics^b							
Q_g	Total Gate Charge	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V},$ $I_{DS} = 30\text{ A}$	-	61	-	nC	Fig.9
Q_{gs}	Gate-Source Charge		-	6	-		
Q_{gd}	Gate-Drain Charge		-	26	-		
$V_{plateau}$	Gate plateau voltage		-	3.0	-		

Notes :

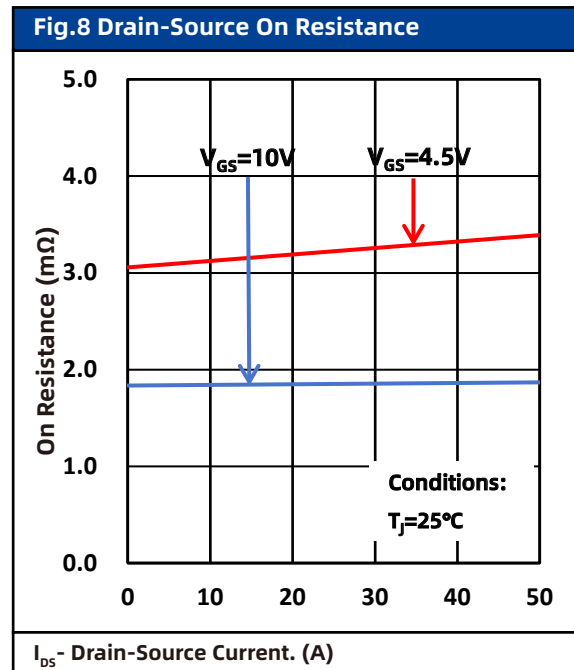
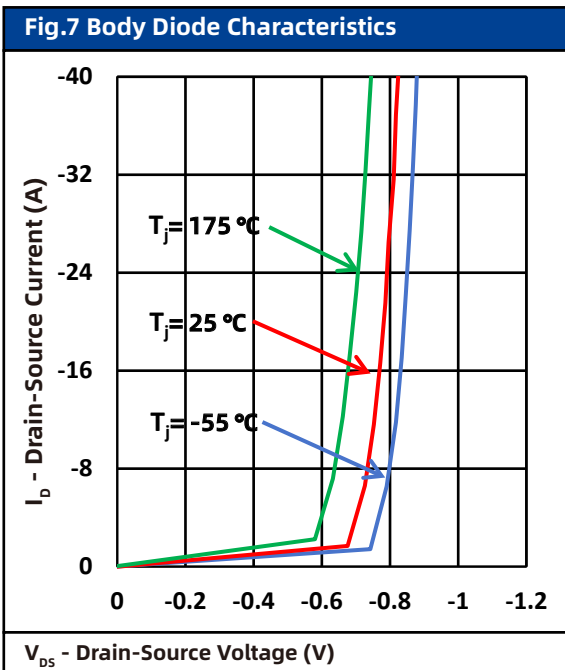
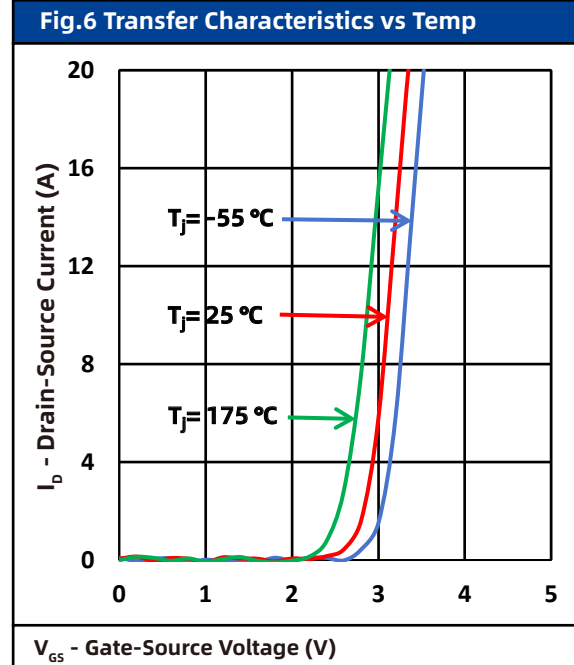
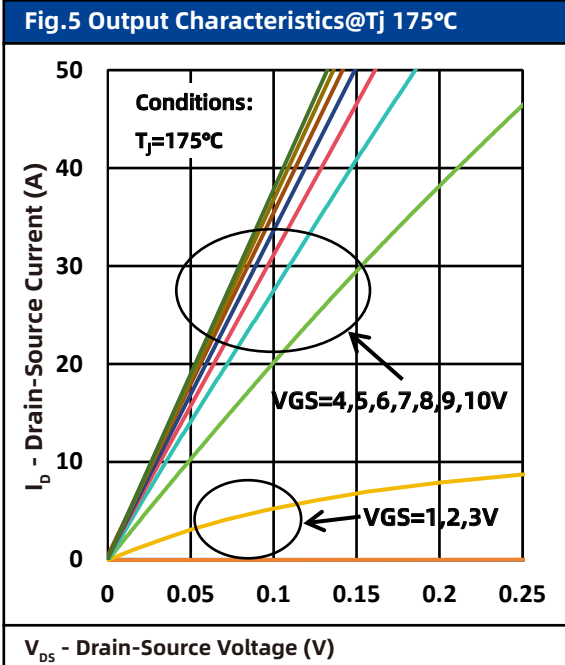
a : Pulse test ; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

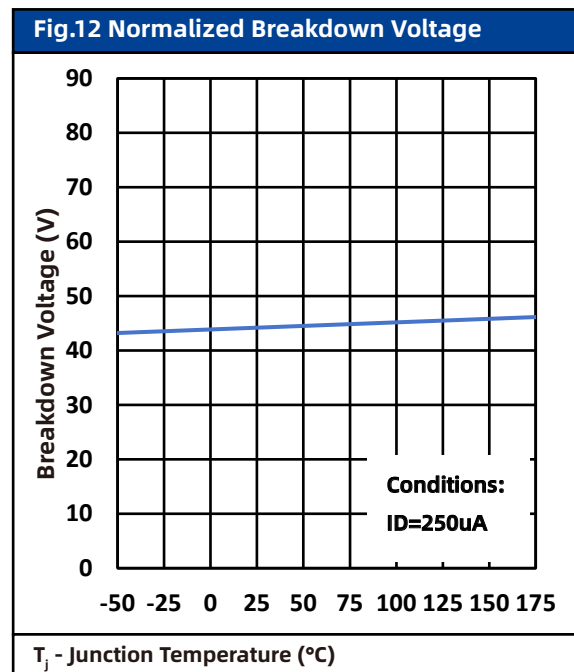
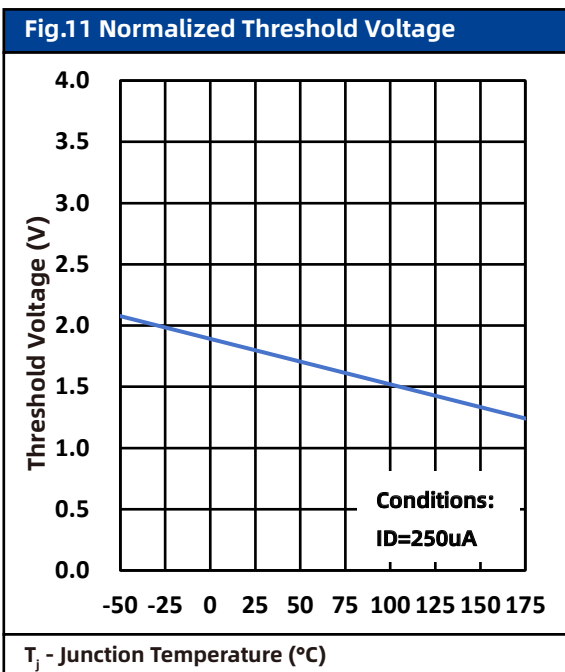
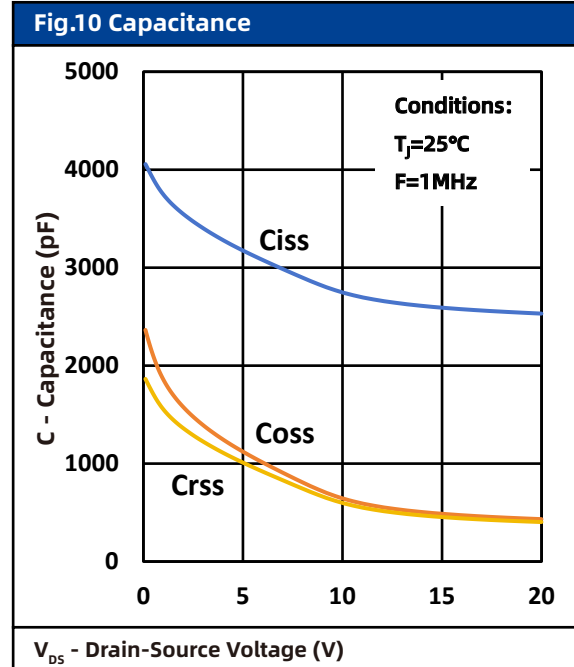
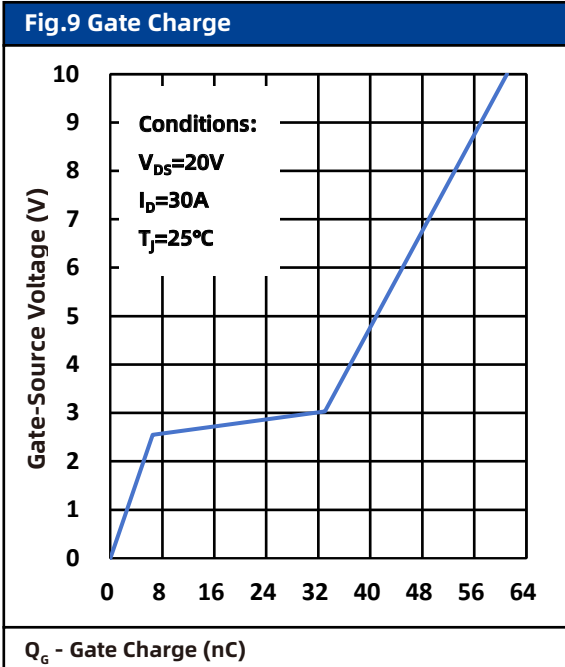
7. Typical Characteristics



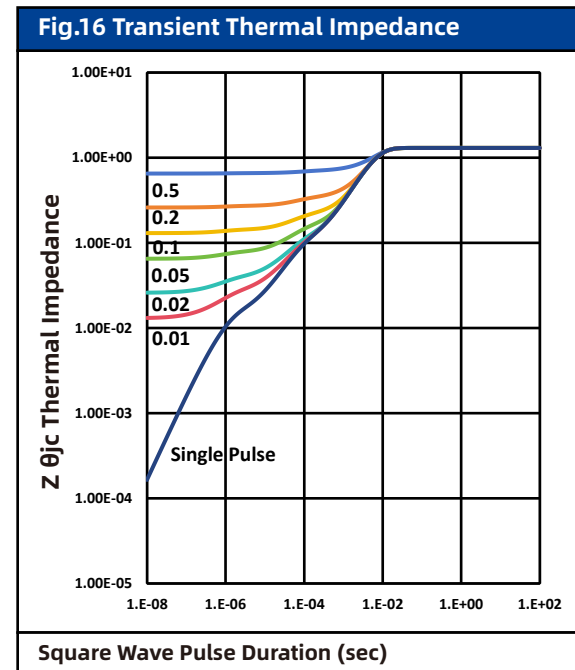
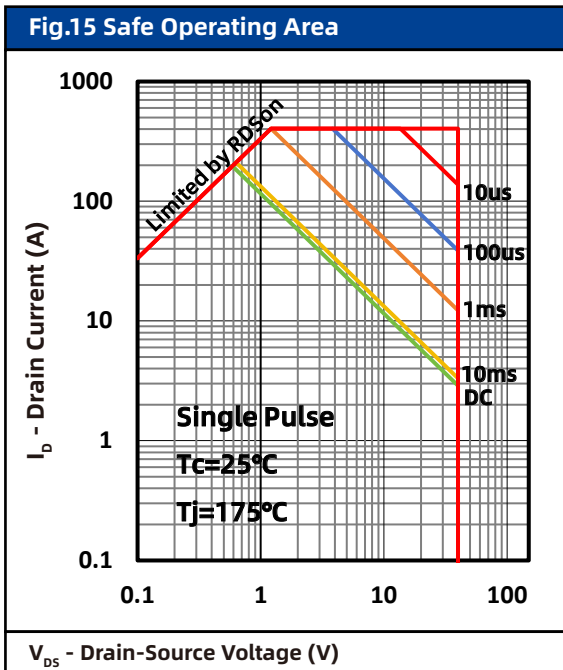
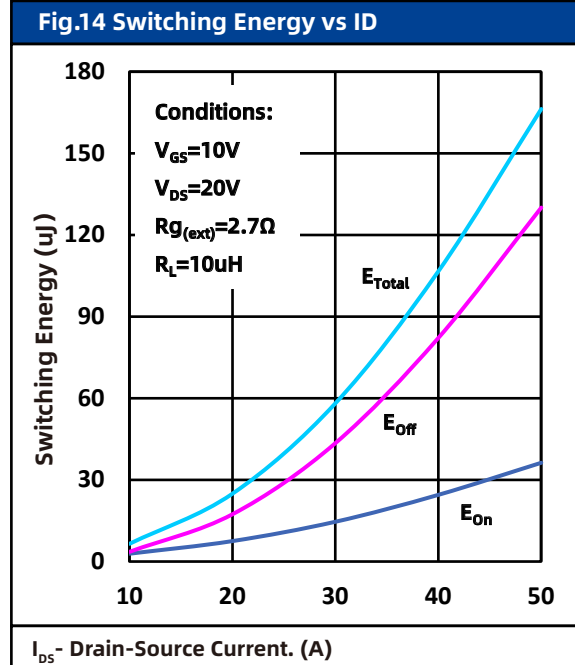
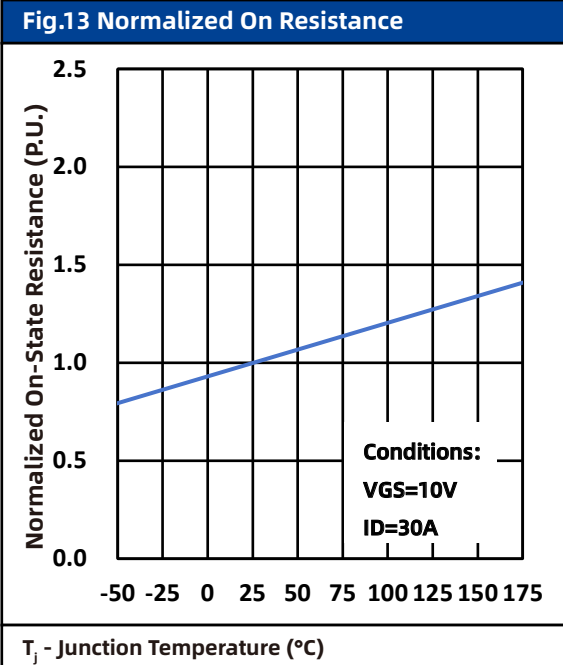
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Fig.17 Gate Charge Test Circuit & Waveform

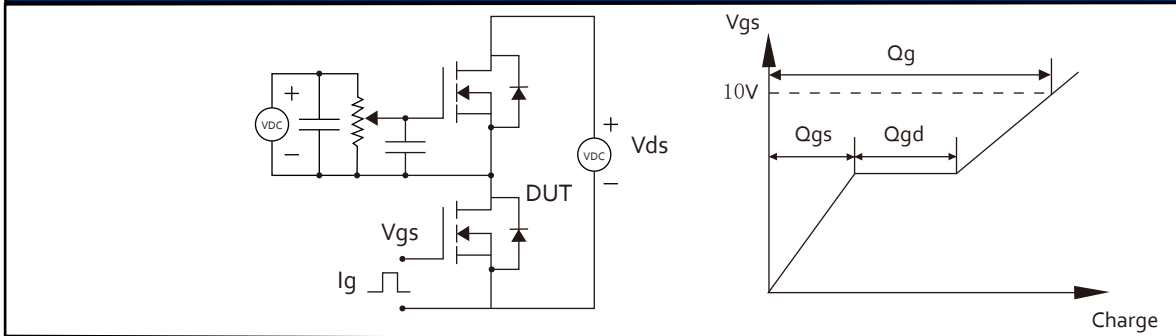


Fig.18 Resistive Switching Test Circuit & Waveforms

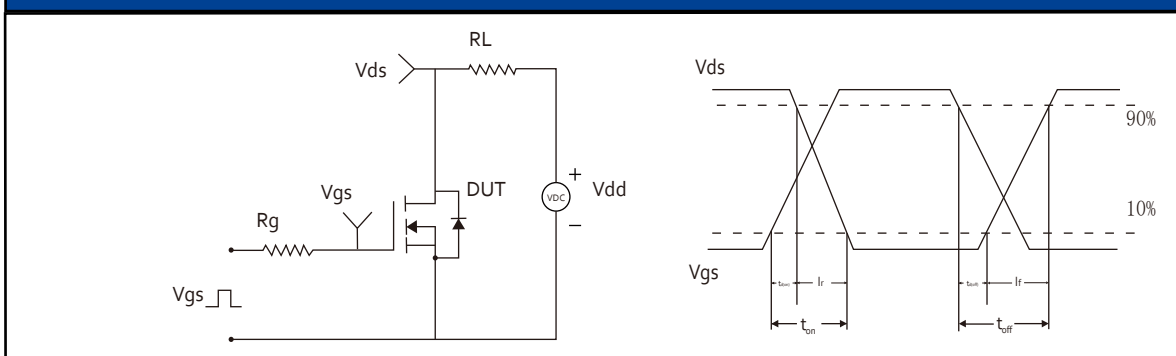


Fig.19 Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

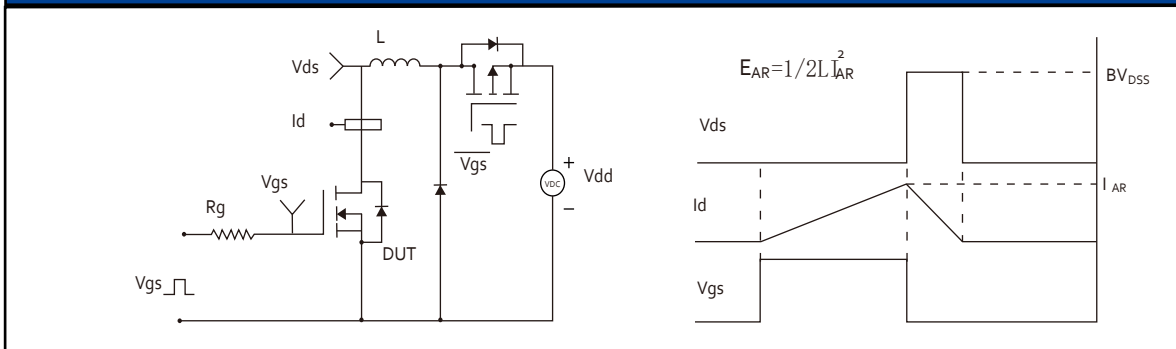
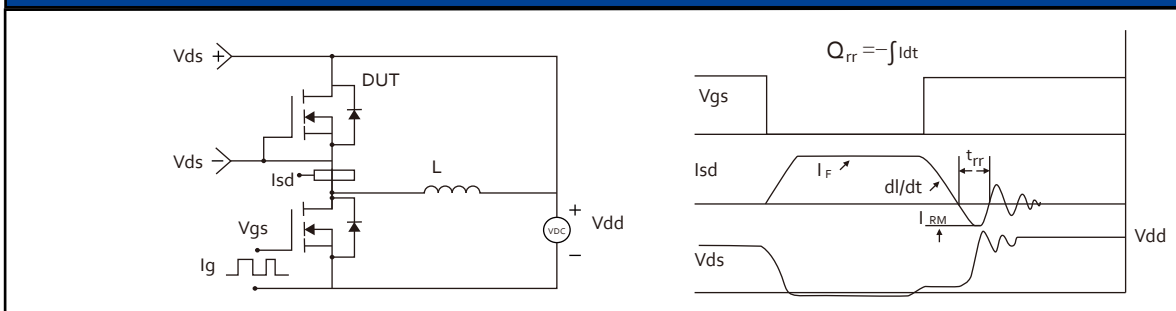
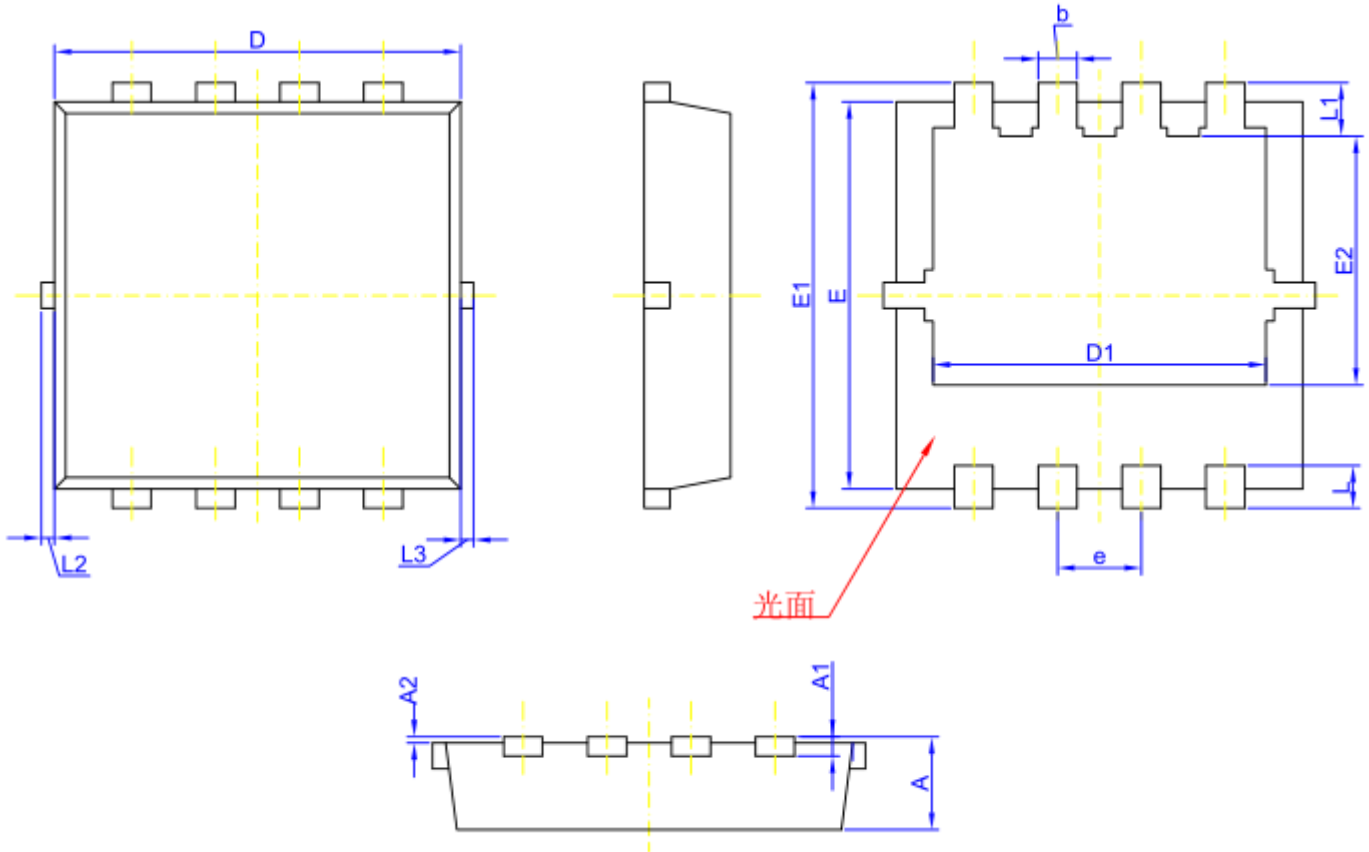


Fig.20 Diode Recovery Test Circuit & Waveforms



8. Package Dimensions

PDFN3.3*3.3 Package



Symbol	Dimensions In Millimeters		
	MIN.	NOM.	MAX.
A	0.700	0.800	0.900
A1	0.100	0.150	0.200
A2	-	-	0.050
D	3.000	3.100	3.200
D1	2.350	2.450	2.550
E	3.000	3.100	3.200
E1	3.200	3.400	3.600
E2	1.635	1.735	1.835
b	0.200	0.300	0.400
e	0.550	0.650	0.750
L	0.250	0.450	0.650
L1	0.345	0.545	0.745
L2	0~0.100		
L3	0~0.100		

9. Record of Document amendment

产品名称：LN018N040Q
版权说明：雷诺电子（宁波）有限公司
联系电话：4008887385

文档类型：产品手册
公司主页：www.leinuosemi.com

版本：01
修改记录：
1.初版发行