

100V N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ◇ Advanced SGT cell design
- ◇ Low Gate Charge
- ◇ Low On-Resistance
- ◇ RoHS and Halogen-Free Compliant
- ◇ 100% ΔV_{DS} & UIS & Rg Tested

1.2 Applications

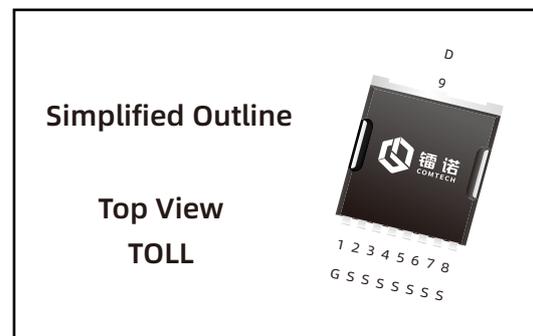
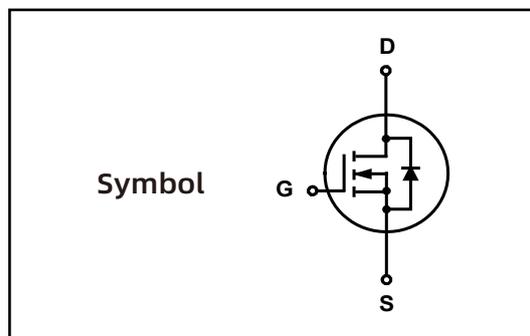
- ◇ DC-DC Converter
- ◇ Drones
- ◇ Motor drivers
- ◇ Light electric vehicles

1.3 Quick reference

- ◇ $BV \cong 100\text{ V}$
- ◇ $P_{\text{tot}} \cong 483\text{ W}$
- ◇ $I_D \cong 500\text{ A}$
- ◇ $R_{DS(ON)} \cong 1.2\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- ◇ $R_{DS(ON)} \cong 2.0\text{ m}\Omega @ V_{GS} = 6\text{ V}$



2. Pin Description



3.Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit	Note
V_{DS}	Drain-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	100	V	-
V_{GS}	Gate-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	± 20	V	-
I_D^*	Drain Current (DC)	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	500	A	Fig.2
		$T_C = 100\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	354	A	
$I_{DM}^{**},^{***}$	Drain Current (Pulsed)	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	649	A	-
P_{tot}	Drain power dissipation	$T_C = 25\text{ }^\circ\text{C}$	-	483	W	Fig.1
		$T_C = 100\text{ }^\circ\text{C}$	-	241	W	
T_{stg}	Storage Temperature		-55	175	$^\circ\text{C}$	-
T_J	Junction Temperature		-	175	$^\circ\text{C}$	-
I_S	Continuous-Source Current	$T_C = 25\text{ }^\circ\text{C}$	-	500	A	-
E_{AS}^*	Single Pulsed Avalanche Energy	$V_{DD} = 100\text{ V}, L = 0.1\text{ mH}$	-	831	mJ	Fig.19

4.Thermal Characteristics

$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient	-	14	$^\circ\text{C}/\text{W}$	Fig.16
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case	-	0.31		

Notes :

- * Surface Mounted on 1 in² pad area, $t \leq 10\text{ sec}$
- ** Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- *** limited by bonding wire

5.Marking Information

Product Name	Package	Reel size	Tape width	Quantity	Note
LN009N100TP	TOLL	330mm	24mm	2000	

Note: COMTECH defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

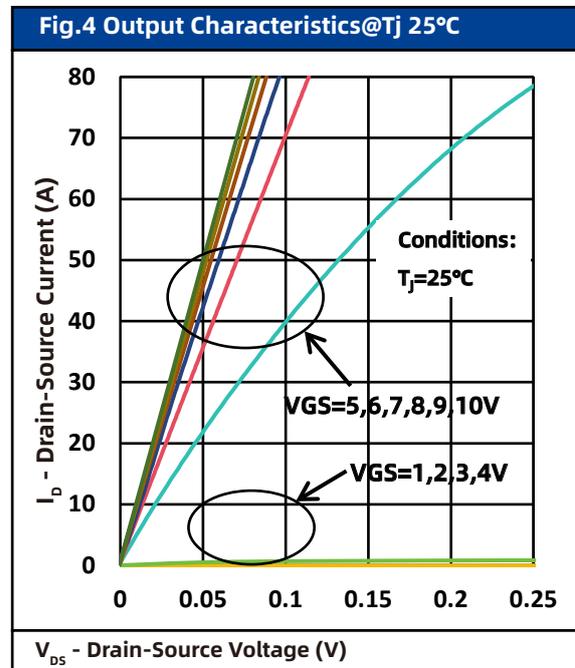
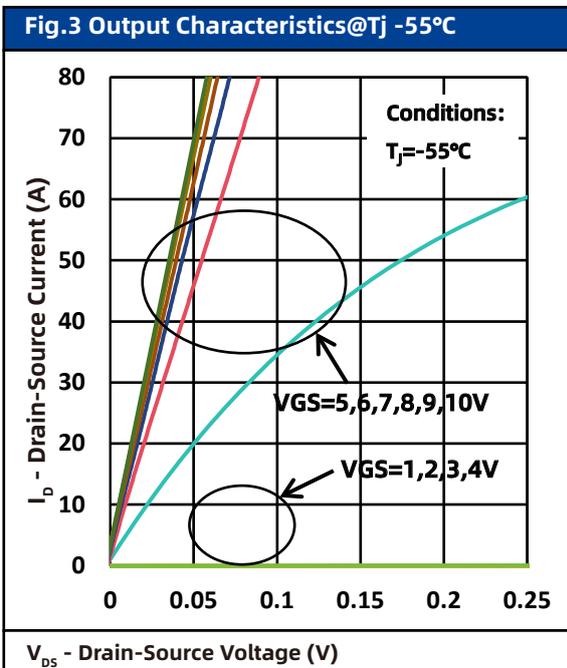
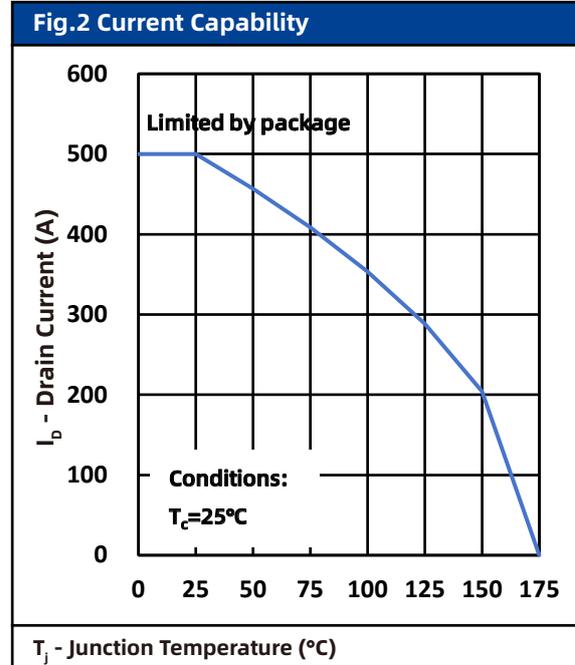
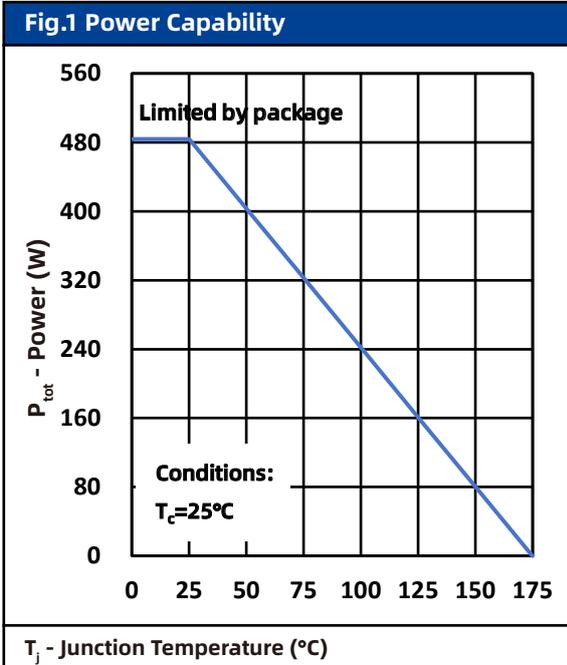
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
Static Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	100	-	-	V	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	2	-	4	V	
I_{DSS}	Drain Leakage Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA	
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA	
$R_{DS(on)}^a$	On-State Resistance	$V_{GS} = 10\text{ V}, I_{DS} = 50\text{ A}$	-	1.0	1.2	m Ω	Fig.8
		$V_{GS} = 6\text{ V}, I_{DS} = 30\text{ A}$	-	1.5	2.0		
Diode Characteristics							
V_{SD}^a	Diode Forward Voltage	$I_{SD} = 50\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V	Fig.7
t_{rr}	Reverse Recovery Time	$I_{DS} = 50\text{ A}, V_{GS} = 0\text{ V}$	-	55	-	nS	Fig.20
Q_{rr}	Reverse Recovery Charge	$dI_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	497	-	nC	
Dynamic Characteristics^b							
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$ Frequency = 1 MHz	-	13332	-	pF	Fig.10
C_{OSS}	Output Capacitance		-	5292	-		
C_{rSS}	Reverse Transfer Capacitance		-	130	-		
R_G	Gate Resistance	F = 1 MHz	-	2.1	-	Ω	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V},$ $R_G = 2.7\ \Omega, R_L = 4\ \mu\text{H},$ $I_{DS} = 50\text{ A}$	-	46	-	nS	Fig.18
t_r	Turn-on Rise Time		-	76	-		
$t_d(off)$	Turn-off Delay Time		-	71	-		
t_f	Turn-off Fall Time		-	32	-		
dv/dt	Peak Diode Recovery		-	0.523	-		
di/dt	Peak Diode Recovery	-	1113	-	A/ μs		
Gate Charge Characteristics^b							
Q_g	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V},$ $I_{DS} = 50\text{ A}$	-	164	-	nC	Fig.9
Q_{gs}	Gate-Source Charge		-	48	-		
Q_{gd}	Gate-Drain Charge		-	52	-		
$V_{plateau}$	Gate plateau voltage		-	4.9	-		

Notes :

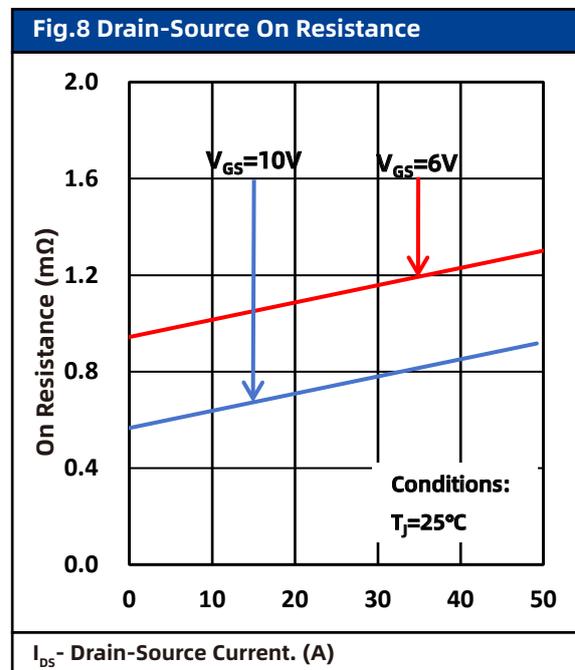
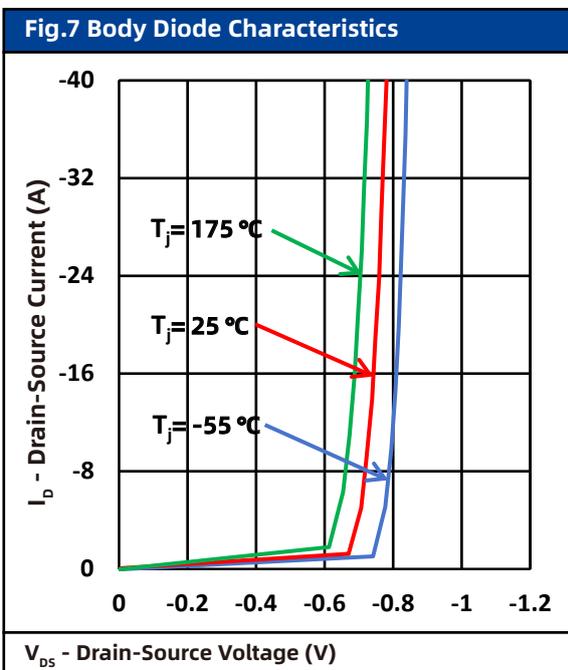
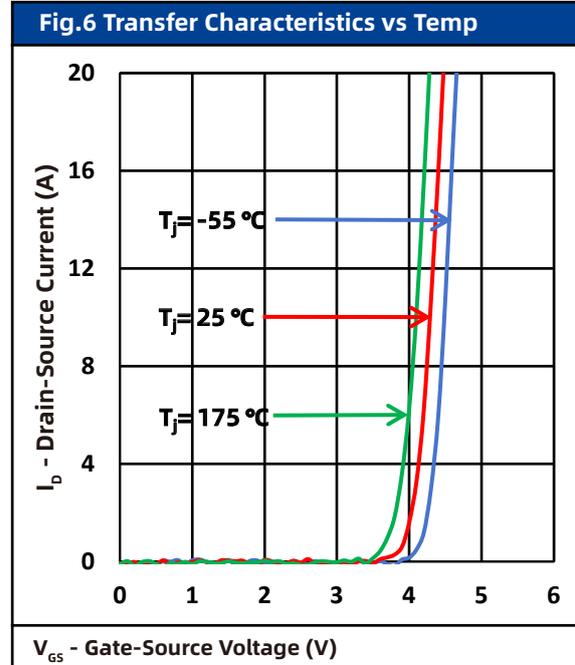
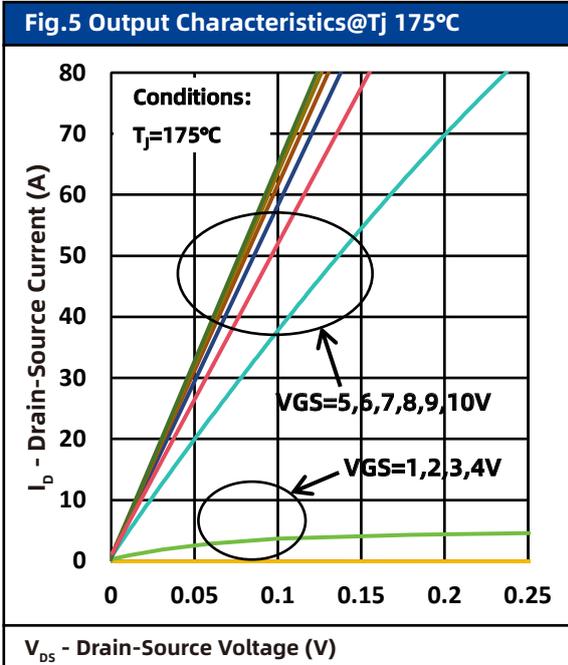
a : Pulse test ; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

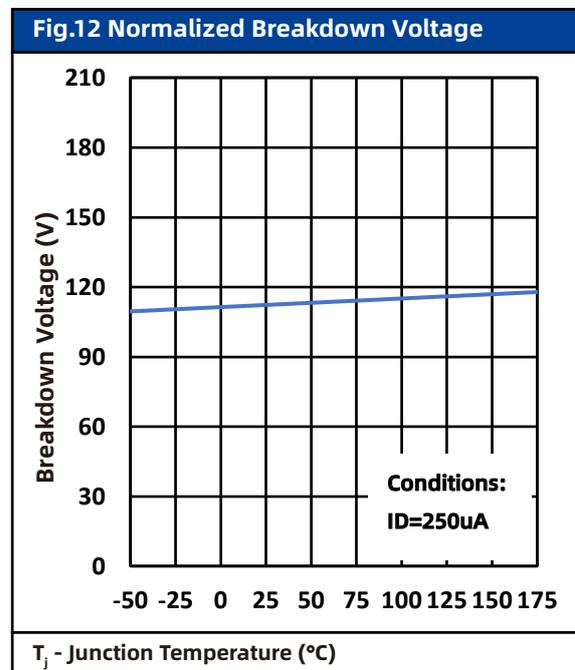
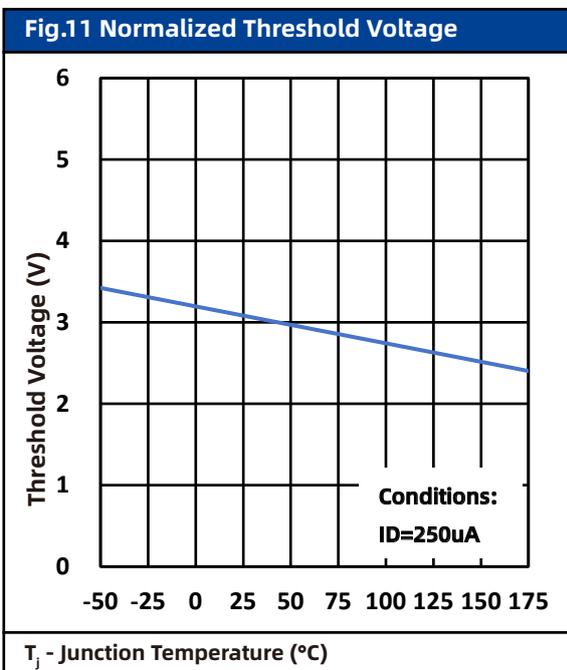
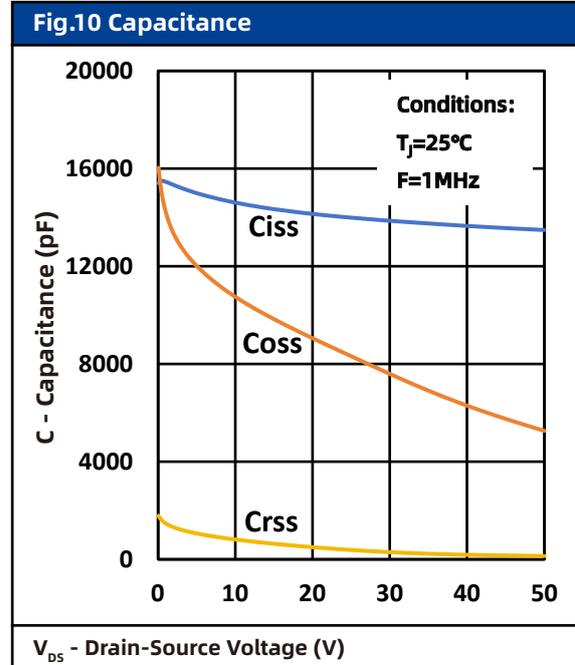
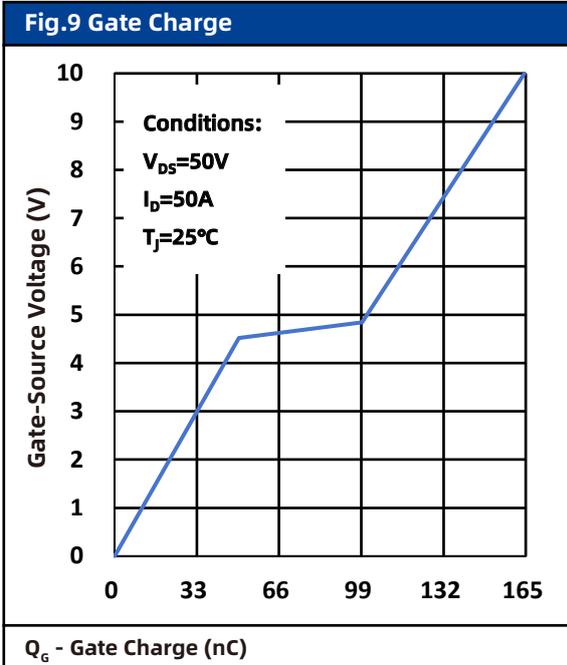
7. Typical Characteristics



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Fig.13 Normalized On Resistance

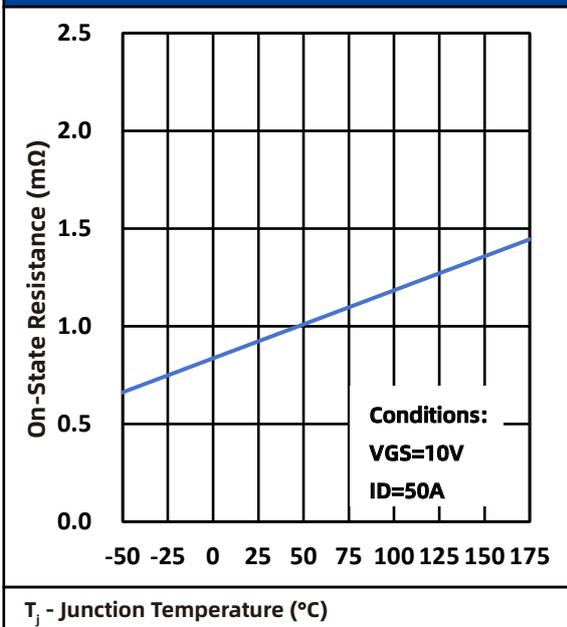


Fig.14 Switching Energy vs ID

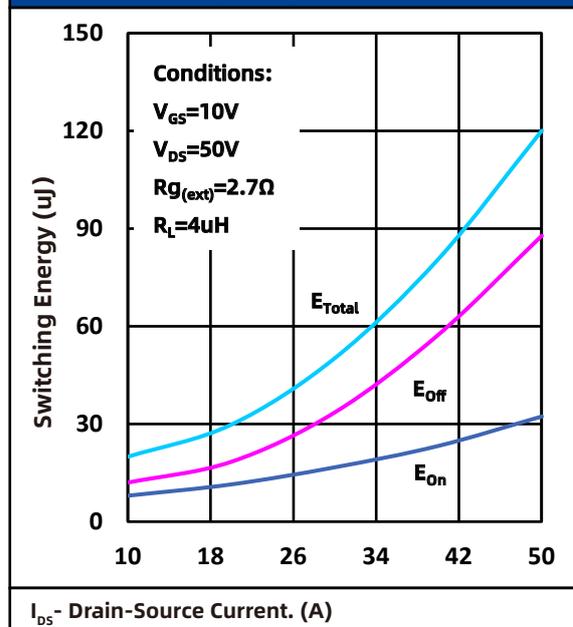


Fig.15 Safe Operating Area

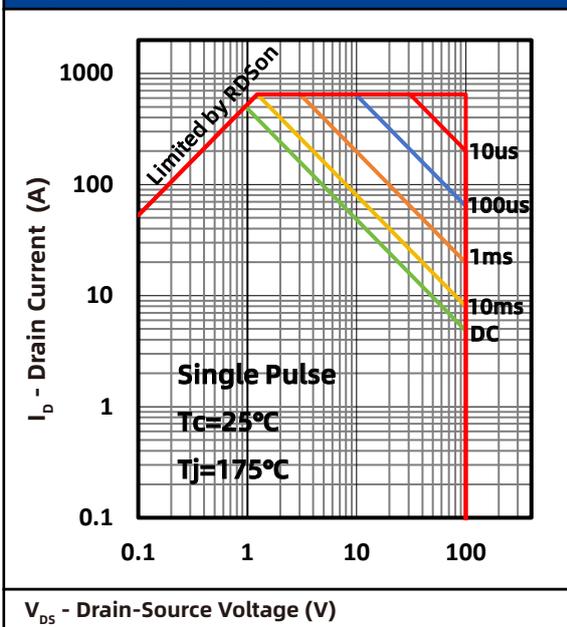
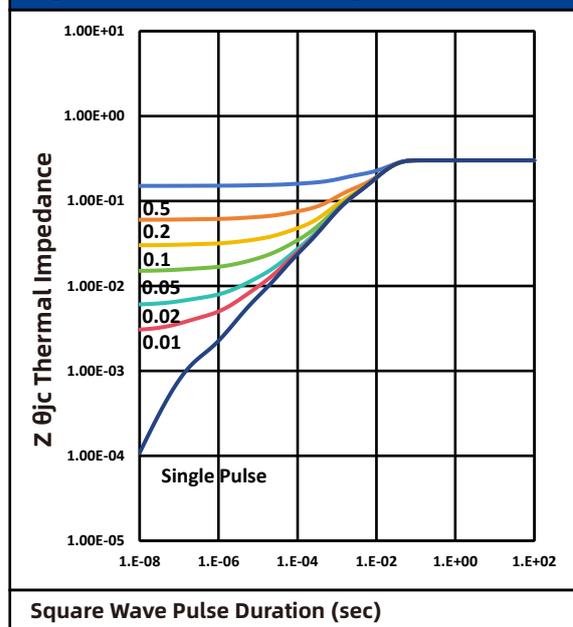


Fig.16 Transient Thermal Impedance



7. Typical Characteristics

Fig.17 Gate Charge Test Circuit & Waveform

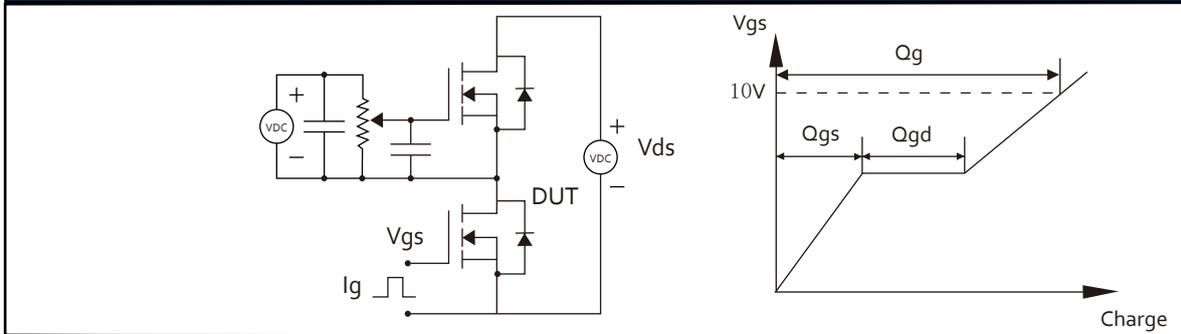


Fig.18 Resistive Switching Test Circuit & Waveforms

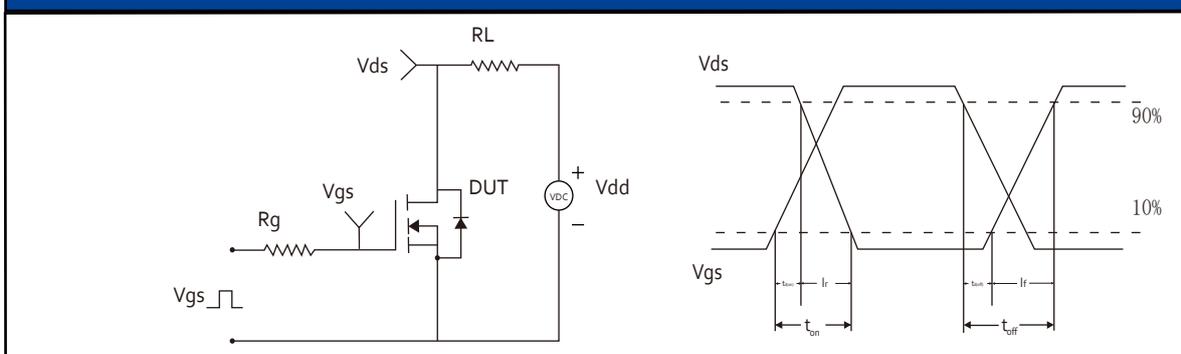


Fig.19 Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

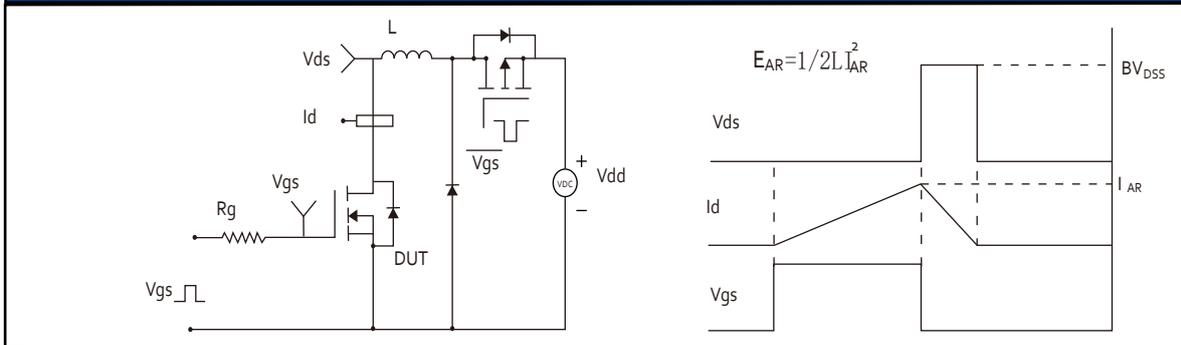
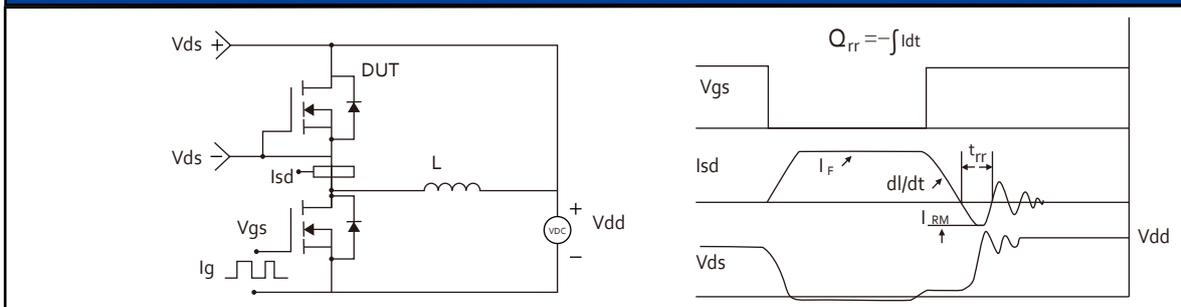
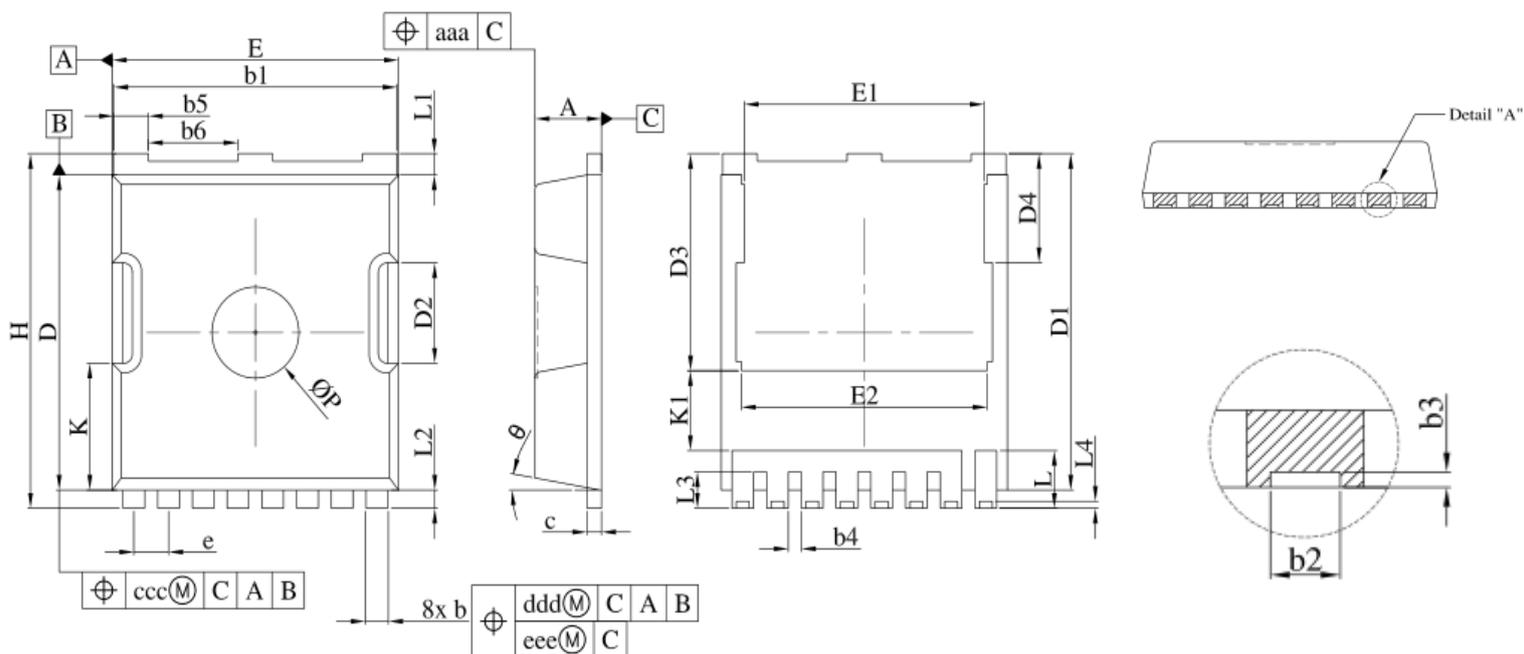


Fig.20 Diode Recovery Test Circuit & Waveforms



8. Package Dimensions

TOLL Package



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.36	0.55
b3	0.05	0.35
b4	0.30	0.50
b5	1.10	1.30
b6	3.00	3.20
c	0.40	0.60
D	10.28	10.55
D1	10.98	11.18
D2	3.20	3.40
D3	7.00	7.30
D4	3.44	3.74
e	1.10	1.30
E	9.80	10.00
E1	8.20	8.40
E2	8.35	8.65
H	11.50	11.85
K	4.08	4.28
K1	2.45	-
L	1.60	2.10
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	0.13	0.33
P	2.85	3.15
θ	10°REF	

9. Record of Document amendment

产品名称：LN009N100TP
版权说明：镭诺电子（宁波）有限公司
联系电话：4008887385

文档类型：产品手册

公司主页：www.leinuosemi.com

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修改记录：
1.初版发行