

## 40V N-Channel Enhancement Mode MOSFET

### 1. Product Information

#### 1.1 Features

- ◇ Advanced SGT cell design
- ◇ Low Gate Charge
- ◇ Low On-Resistance
- ◇ RoHS and Halogen-Free Compliant
- ◇ 100%  $\Delta V_{DS}$  & UIS & Rg Tested

#### 1.2 Applications

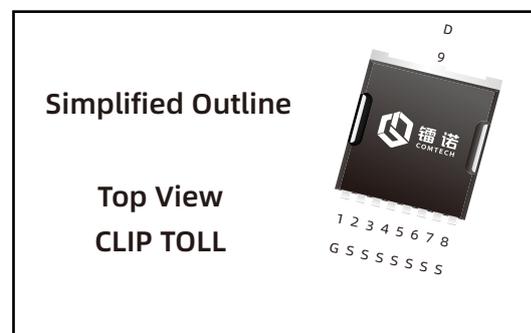
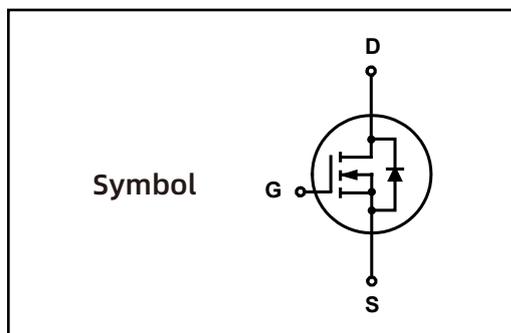
- ◇ DC-DC Converter
- ◇ Drones
- ◇ Motor drivers
- ◇ Light electric vehicles

#### 1.3 Quick reference

- ◇  $BV \cong 40\text{ V}$
- ◇  $P_{\text{tot}} \cong 400\text{ W}$
- ◇  $I_D \cong 500\text{ A}$
- ◇  $R_{DS(ON)} \cong 0.27\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- ◇  $R_{DS(ON)} \cong 0.55\text{ m}\Omega @ V_{GS} = 6\text{ V}$



### 2. Pin Description



## 3.Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit	Note
$V_{DS}$	Drain-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	40	V	-
$V_{GS}$	Gate-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	$\pm 20$	V	-
$I_D^*$	Drain Current ( DC )	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	1000	A	Fig.2
		$T_C = 100\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	707	A	
$I_{DM}^{**},^{***}$	Drain Current ( Pulsed )	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	2476	A	-
$P_{tot}$	Drain power dissipation	$T_C = 25\text{ }^\circ\text{C}$	-	400	W	Fig.1
		$T_C = 100\text{ }^\circ\text{C}$	-	200	W	
$T_{stg}$	Storage Temperature		-55	175	$^\circ\text{C}$	-
$T_J$	Junction Temperature		-	175	$^\circ\text{C}$	-
$I_S$	Continuous-Source Current	$T_C = 25\text{ }^\circ\text{C}$	-	1000	A	-
$E_{AS}^*$	Single Pulsed Avalanche Energy	$V_{DD} = 40\text{ V}, L = 0.5\text{ mH}$	-	5256	mJ	Fig.19

## 4.Thermal Characteristics

$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient	-	24	$^\circ\text{C}/\text{W}$	Fig.16
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case	-	0.28		

Notes :

\* Surface Mounted on 1 in<sup>2</sup> pad area,  $t \leq 10\text{ sec}$

\*\* Pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$

\*\*\* limited by bonding wire

## 5.Marking Information

Product Name	Package	Reel size	Tape width	Quantity	Note
LNR20N040CT-H	CLIP TOLL	330mm	12mm	2000	

Note: COMTECH defines " Green " as lead-free ( RoHS compliant ) and halogen free ( Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C )

## 6. Electrical Characteristics ( $T_A=25^\circ$ Unless Otherwise Noted )

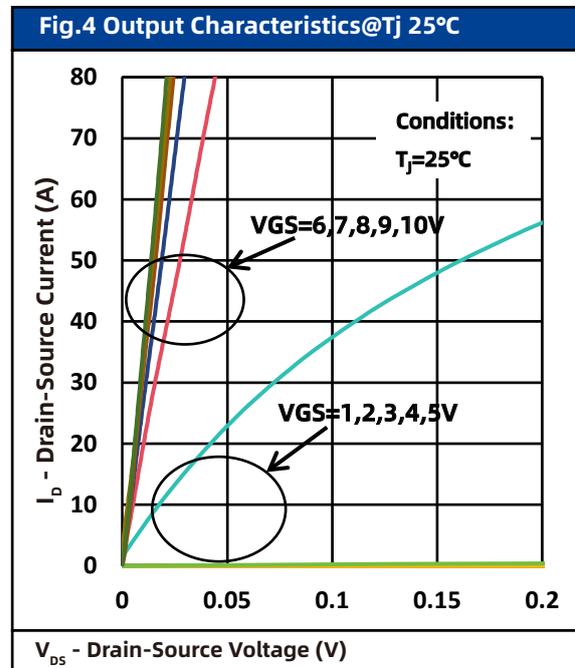
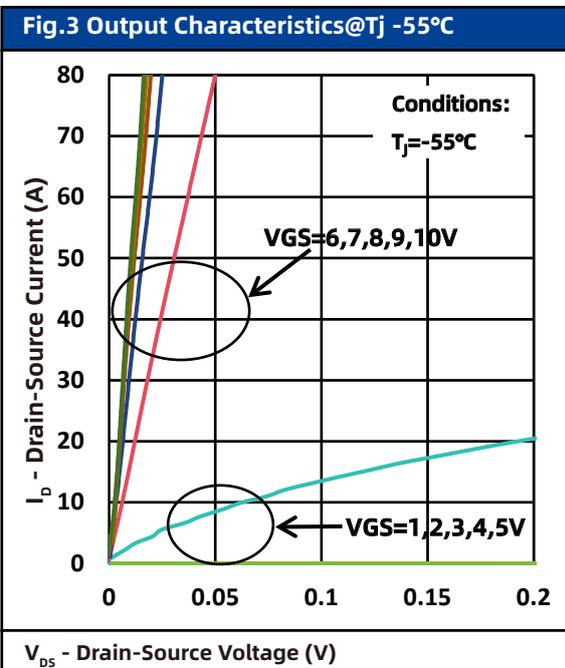
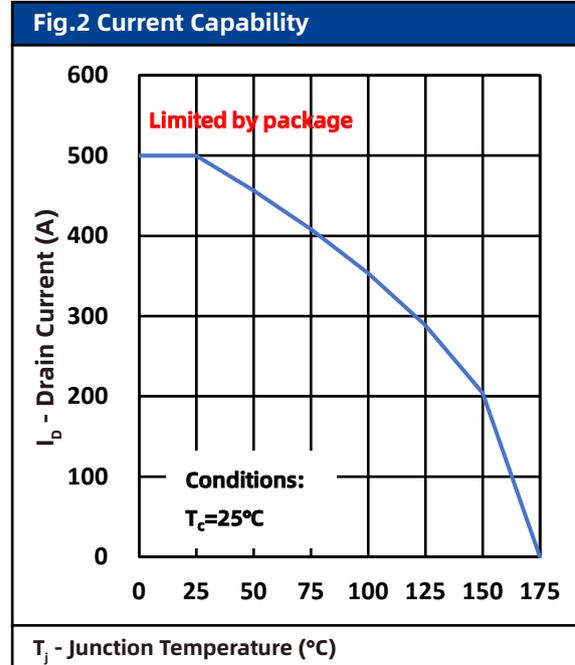
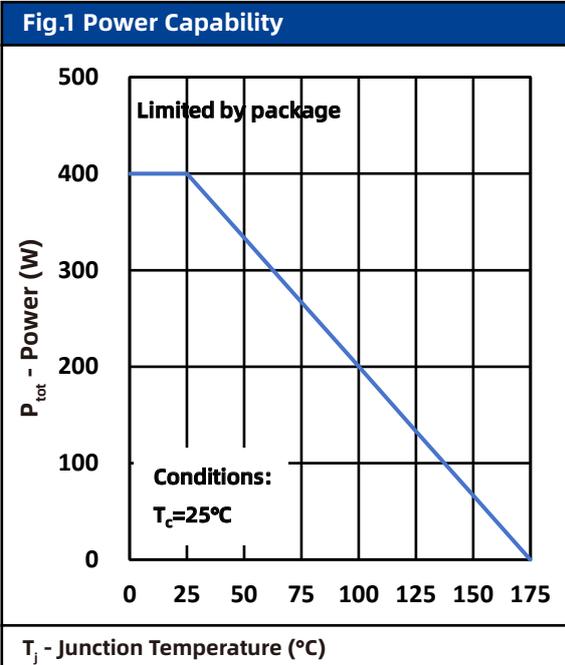
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
<b>Static Characteristics</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	40	-	-	V	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	2	-	4	V	
$I_{DSS}$	Drain Leakage Current	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$	
$I_{GSS}$	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA	
$R_{DS(on)}^a$	On-State Resistance	$V_{GS} = 10\text{ V}, I_{DS} = 50\text{ A}$	-	0.24	0.27	m $\Omega$	Fig.8
		$V_{GS} = 6\text{ V}, I_{DS} = 30\text{ A}$	-	0.45	0.55		
<b>Diode Characteristics</b>							
$V_{SD}^a$	Diode Forward Voltage	$I_{SD} = 50\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V	Fig.7
$t_{rr}$	Reverse Recovery Time	$I_{DS} = 50\text{ A}, V_{GS} = 0\text{ V}$ $dI_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	100	-	nS	Fig.20
$Q_{rr}$	Reverse Recovery Charge		-	268	-	nC	
<b>Dynamic Characteristics<sup>b</sup></b>							
$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$ Frequency = 1 MHz	-	14308	-	pF	Fig.10
$C_{OSS}$	Output Capacitance		-	7436	-		
$C_{rSS}$	Reverse Transfer Capacitance		-	721	-		
$R_G$	Gate Resistance	F= 1 MHz	-	3.9	-	$\Omega$	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V},$ $R_G=2.8\ \Omega, R_L = 8\ \mu\text{H},$ $I_{DS} = 50\text{ A}$	-	43	-	nS	Fig.18
$t_r$	Turn-on Rise Time		-	226	-		
$t_d(off)$	Turn-off Delay Time		-	185	-		
$t_f$	Turn-off Fall Time		-	150	-		
$dv/dt$	Peak Diode Recovery		-	0.071	-		
$di/dt$	Peak Diode Recovery	-	241	-	A/ $\mu\text{s}$		
<b>Gate Charge Characteristics<sup>b</sup></b>							
$Q_g$	Total Gate Charge	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V},$ $I_{DS} = 50\text{ A}$	-	308	-	nC	Fig.9
$Q_{gs}$	Gate-Source Charge		-	73	-		
$Q_{gd}$	Gate-Drain Charge		-	109	-		
$V_{plateau}$	Gate plateau voltage		-	4.4	-		

Notes :

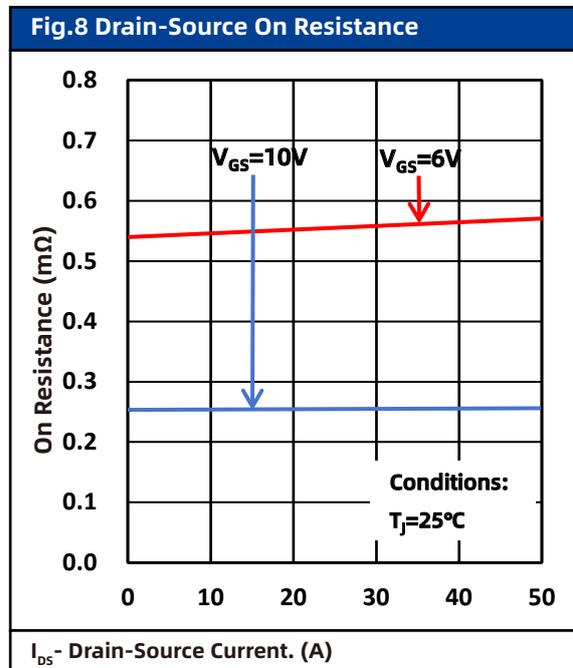
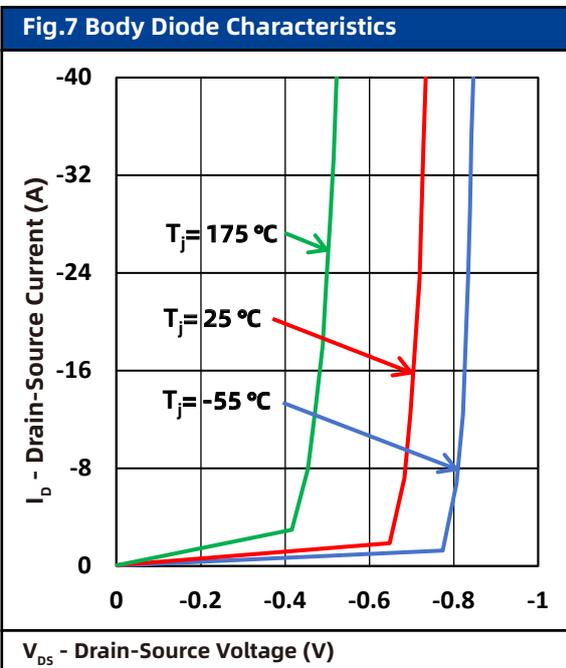
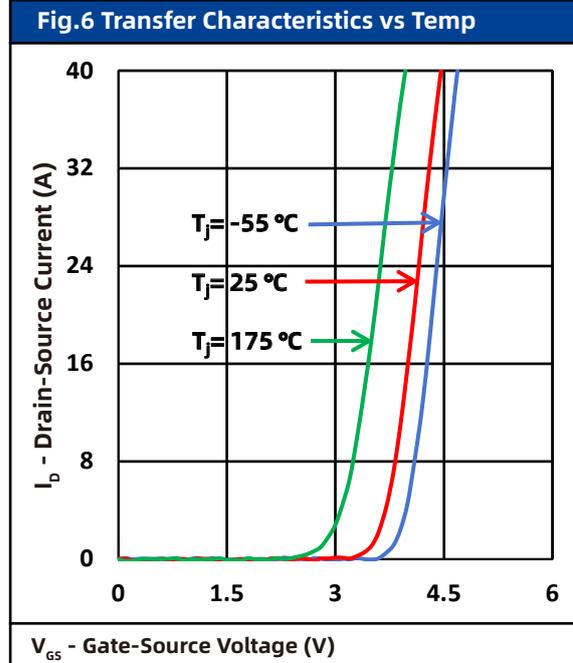
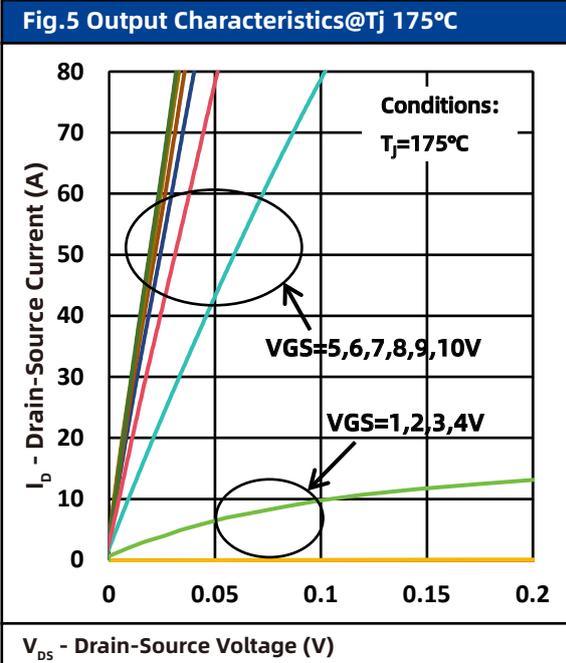
a : Pulse test ; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$

b : Guaranteed by design, not subject to production testing

## 7. Typical Characteristics



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Fig.9 Gate Charge

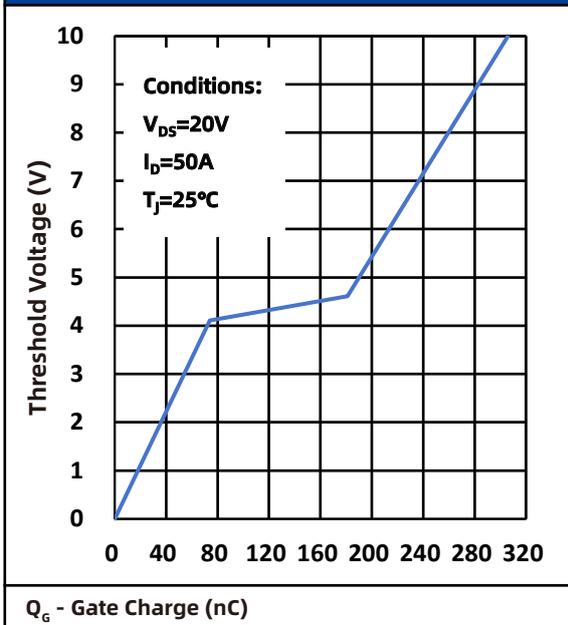


Fig.10 Capacitance

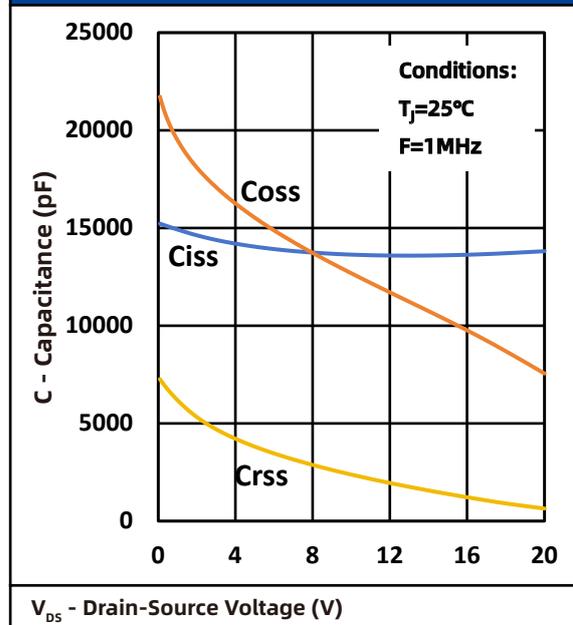


Fig.11 Normalized Threshold Voltage

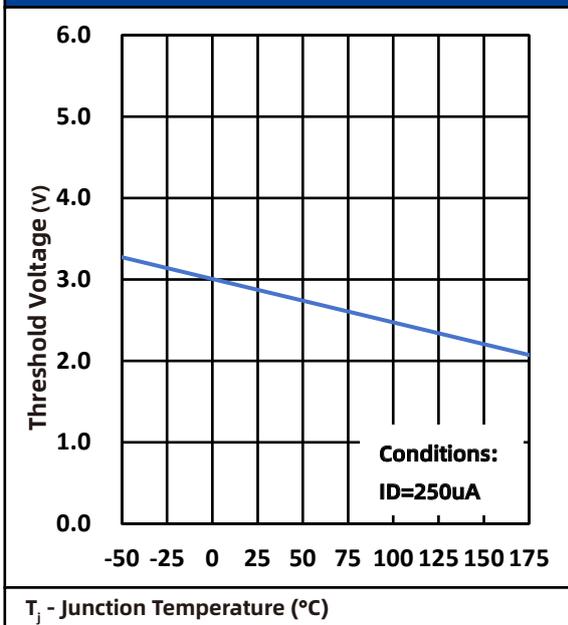
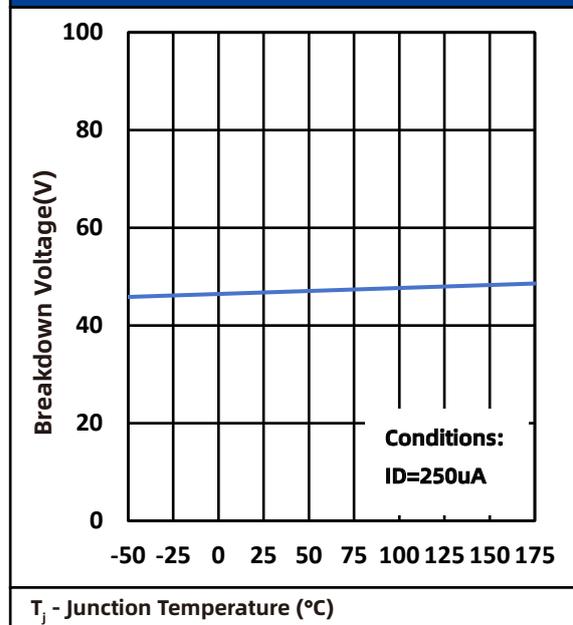
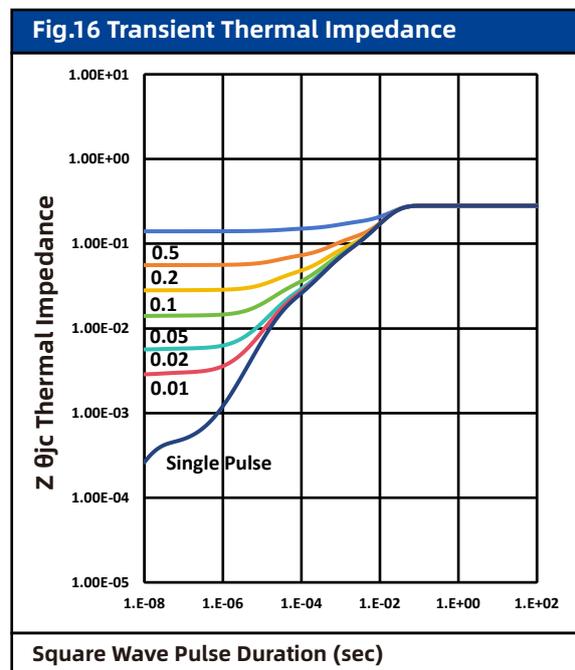
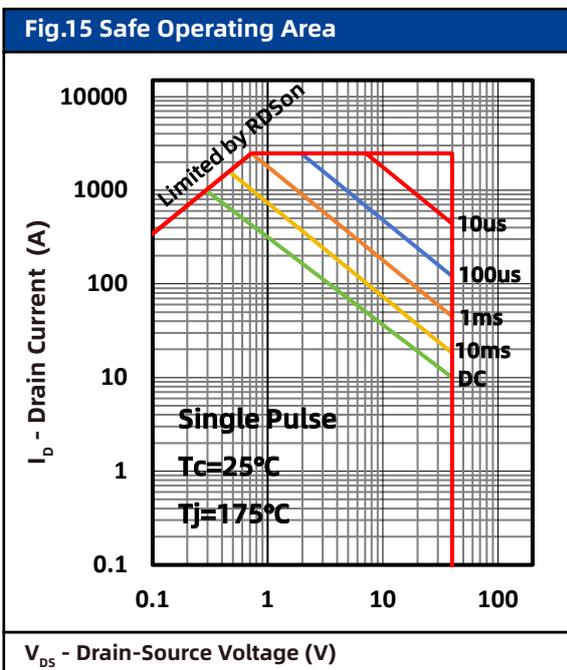
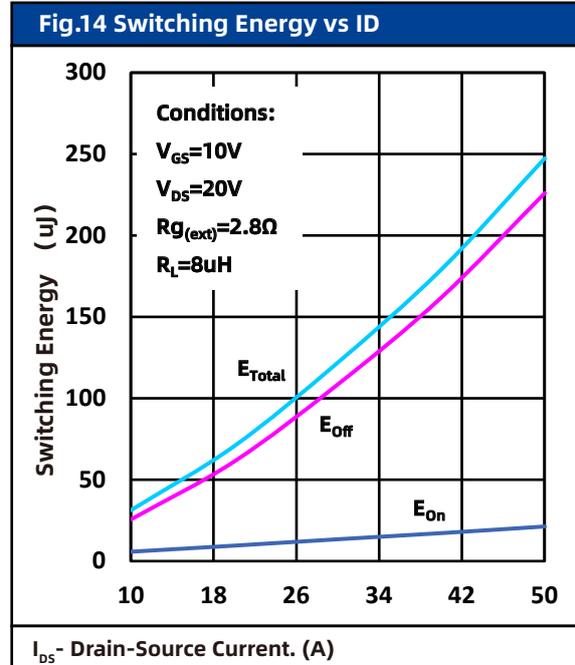
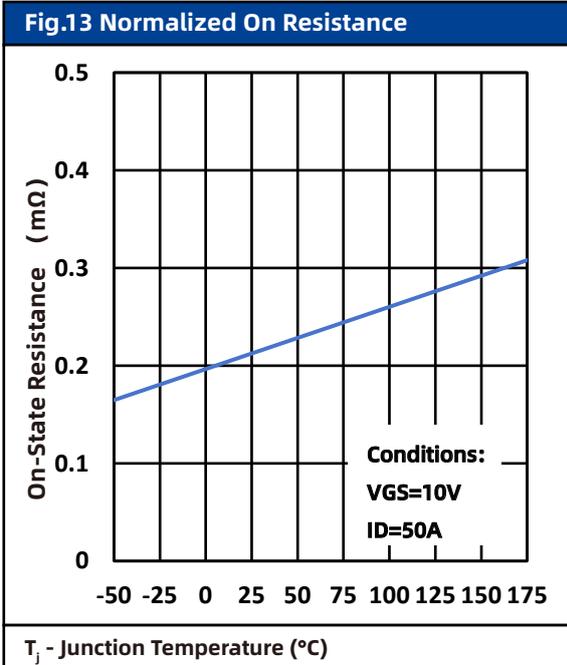


Fig.12 Normalized Breakdown Voltage



## 7. Typical Characteristics



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Fig.17 Gate Charge Test Circuit & Waveform

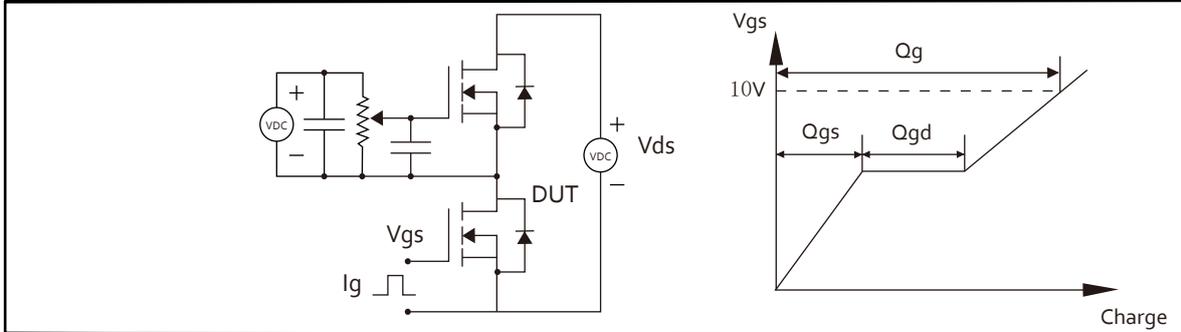


Fig.18 Resistive Switching Test Circuit & Waveforms

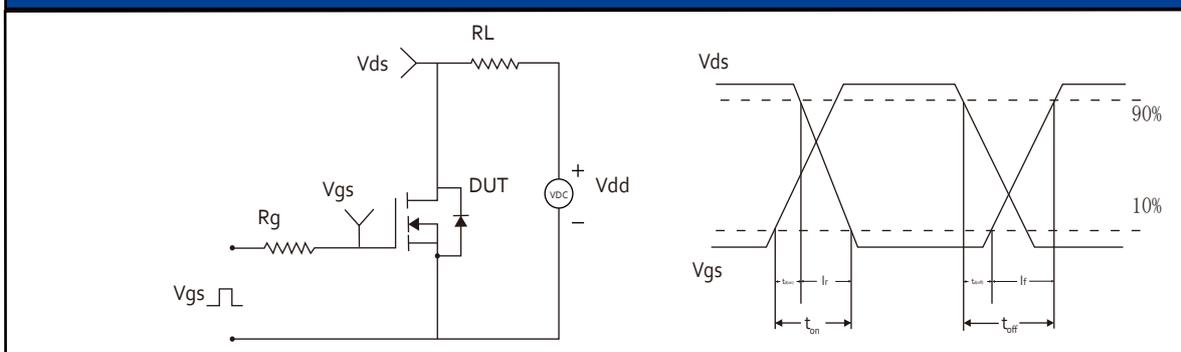


Fig.19 Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

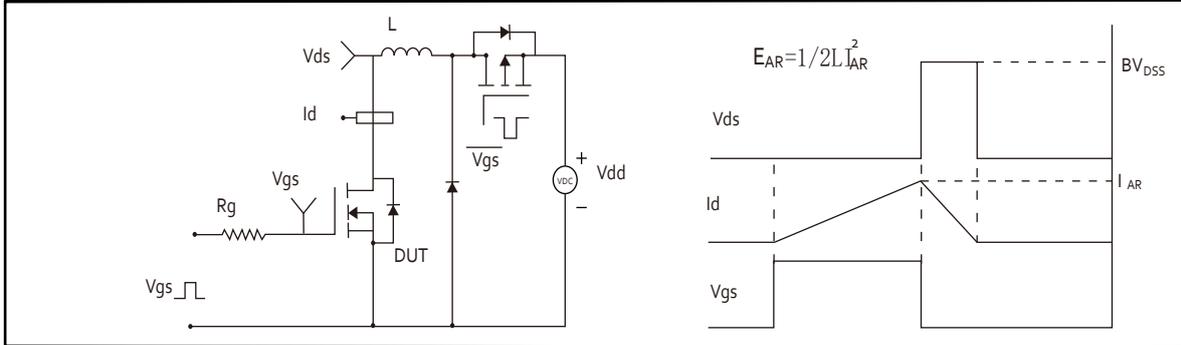
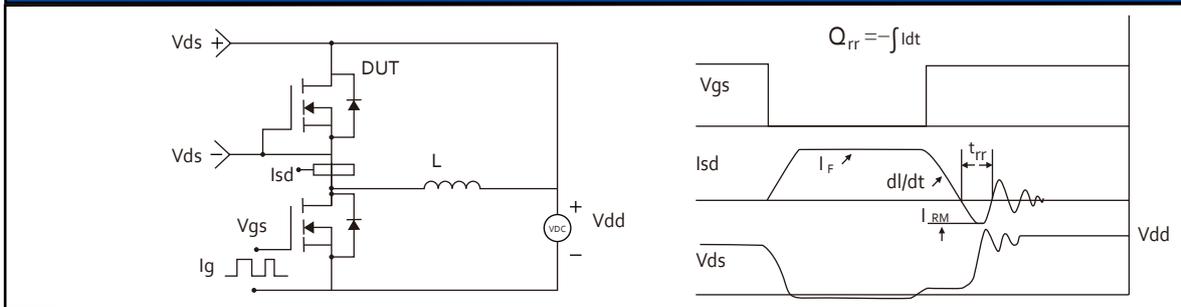
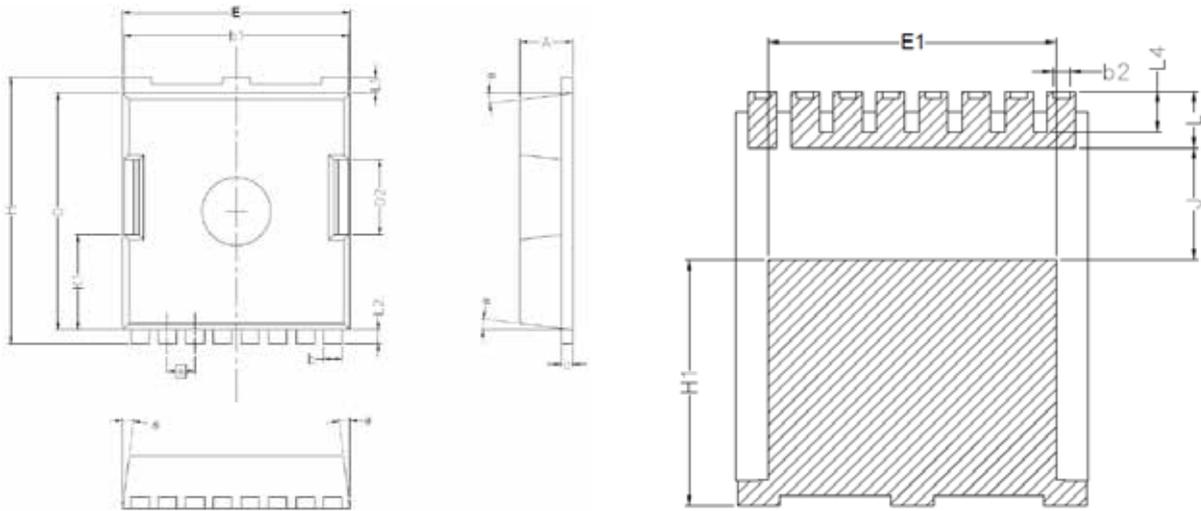


Fig.20 Diode Recovery Test Circuit & Waveforms



## 8. Package Dimensions

### CLIP TOLL Package



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.10
E1	7.90	8.30
e	1.20BSC	
H	11.48	11.88
H1	6.75	7.15
N	8	
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
$\theta$	4°	10°

## 9. Record of Document amendment

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联系电话：4008887385

文档类型：产品手册

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修改记录：  
1.初版发行